XAPP696 (v1.3) May 1, 2008

Interfacing LVPECL 3.3V Drivers with Xilinx 2.5V Differential Receivers

Author: Mark Wood

Summary

This application note describes how to interface 3.3V differential Low-Voltage Positive Emitter Coupled Logic (LVPECL) drivers with Xilinx® 2.5V differential receivers, including Virtex®-II Pro, Virtex-II Pro X, Virtex-4, Virtex-5, Spartan®-3E, and Spartan-3 FPGA 2.5V LVPECL and Low Voltage Differential Signaling (LVDS). Several interface modifications are presented with supporting IBIS simulation results. By reducing the 3.3V LVPECL common mode voltage, it is safe to interface with Virtex-II Pro through Virtex-5 and Spartan-3/3E FPGA 2.5V LVPECL and LVDS receivers (and future Xilinx devices that support 2.5V differential inputs).

Introduction

Differential 3.3V LVPECL is commonly used for the transmission of high-speed, low-jitter clocks and high bit-rate data. LVPECL offers the advantage of high noise immunity over relatively long interconnects. Differential input buffers configured with Virtex-E and Virtex-II FPGA LVPECL can be directly connected to 3.3V LVPECL drivers from other vendors. However, Virtex-II Pro through Virtex-5 and Spartan-3/3E FPGA differential receivers cannot directly receive 3.3V LVPECL output levels with standard receiver termination. For the Spartan-3A FPGA families, designs should use the 3.3V LVDS and LVPECL input standards.

Virtex-II Pro through Virtex-5 and Spartan-3/3E FPGA Differential 2.5V Input Specification

A standard 2.5V LVPECL interface is shown in Figure 1. The recommended termination technique for interfacing Xilinx differential receivers to 2.5V differential standards is a parallel 100Ω termination between the receiver inputs (as shown in Figure 1). The acceptable input level range for Virtex-II Pro through Virtex-5 and Spartan-3 FPGA differential input receivers is summarized in Table 1. An IBIS simulation of the interface is shown in Figure 2. The driver and receiver used in the simulation were Virtex-II Pro FPGA 2.5V LVPECL, and the receiver voltages were probed at the die pads (see Figure 2 for simulation results).

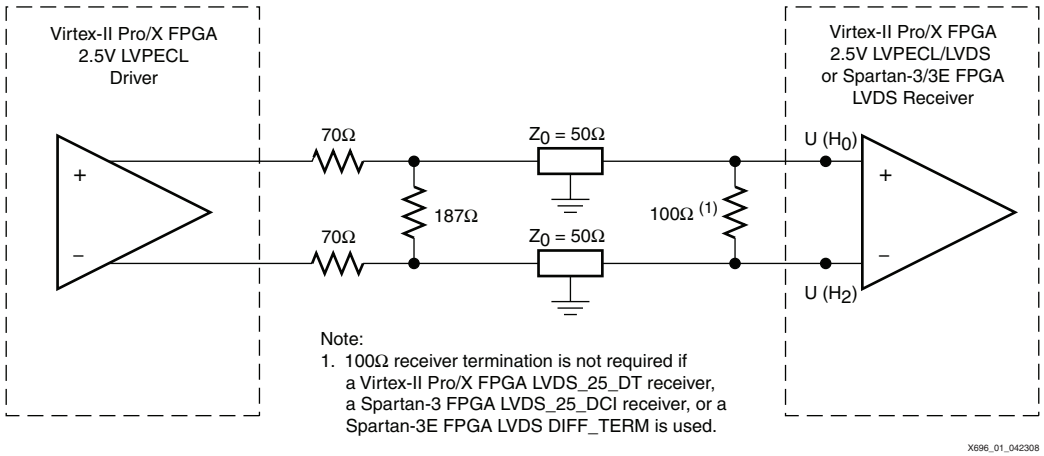

Figure 1: **Virtex-II Pro through Virtex-5 and Spartan-3/3E FPGA 2.5V LVPECL Termination Circuit**

Table 1: **Xilinx Virtex-II Pro through Virtex-5 and Spartan-3 FPGA Differential Receiver DC Levels**

DC Parameter	Symbol	Condition	Min	Typ	Max
Differential Input Voltage (Data Sheet Specification)	V_{IDIFF}	V_{CM} = 1.25V	0.1V		1.0V
Input Common-Mode Voltage (Data Sheet Specification)	V_{ICM}	V_{IDIFF} = ±350 mV	0.3V		2.2V
Simulated Differential Input Voltage	$V_{IDIFFSIM}$	Measured from Figure 2		0.82V	
Simulated Common-Mode Input Voltage	V_{ICMSIM}	Measured from Figure 2		1.2V	

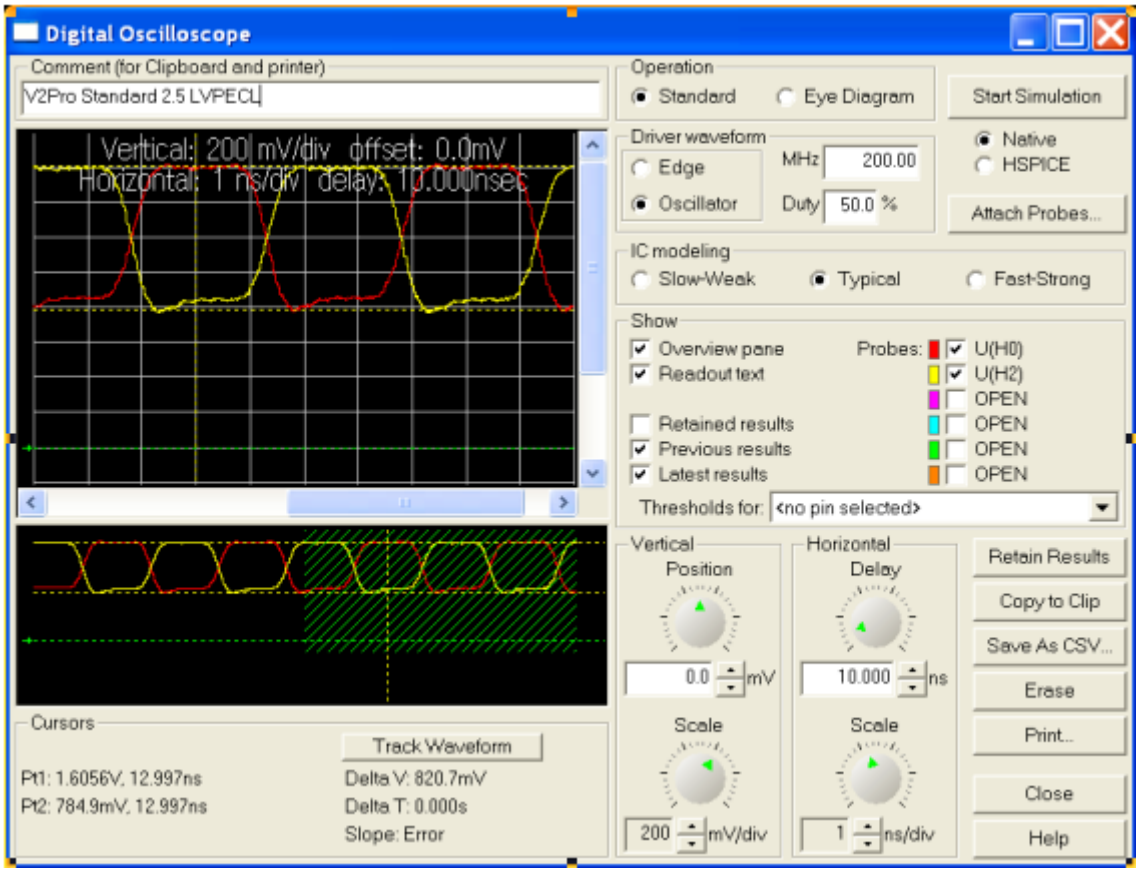

Figure 2: **Virtex-II Pro FPGA 2.5V LVPECL Receiver Voltage Levels**

3.3V LVPECL Output Specification

Many parts used in high-speed transceiver designs use 3.3V LVPECL differential standard I/O. The 3.3V LVPECL output voltage levels vary from vendor to vendor. However, a maximum output level exceeding 2.5V is commonly specified in vendor data sheets. A common termination technique used for 3.3V LVPECL interfaces is shown in Figure 3.

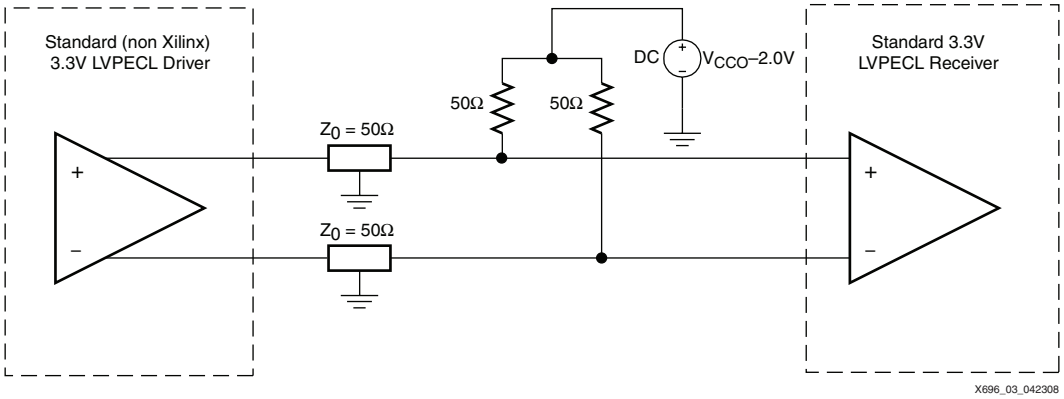

Figure 3: **Standard 3.3V LVPECL Termination**

Interface Modification Advice

When interfacing a 3.3V LVPECL driver to a Virtex-II Pro through Virtex-5 or Spartan-3/3E FPGA 2.5V differential receiver, the output specification for the driver must be considered. If the output levels of the driver are within the Xilinx specified receiver levels, the standard receiver termination can be used. This typically consists of a 100Ω parallel termination, or 50Ω split termination to V_{CCO} – 2.0V.

For driver output levels that exceed the specified receiver input levels, custom termination techniques to reduce the common mode voltage level or the voltage swing can be used.

DC-Coupled Receiver Common Mode Voltage Shift

By replacing the standard receiver termination with a custom termination network, the common mode voltage can be reduced, while maintaining an optimal voltage swing. An example of such a technique is shown in Figure 4. Six termination resistors are required for each differential receiver.

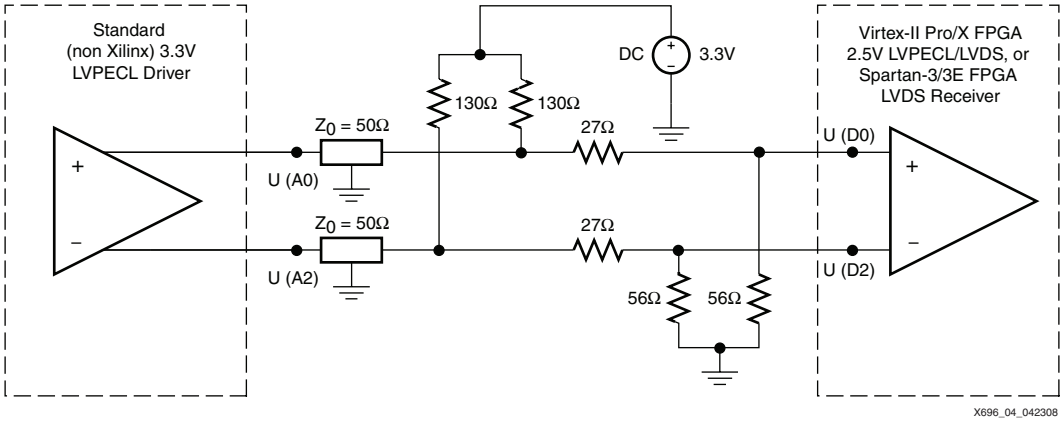

Figure 4: **3.3V LVPECL to 2.5V Differential Receiver DC-Coupled Interface**

The circuit shown in Figure 4 was simulated in IBIS. In the results in Figure 5, the common mode voltage was reduced from approximately 2.25V (at the driver output) to 1.5V (at the receiver input), comfortably meeting the Xilinx Virtex-II Pro through Virtex-5 and Spartan-3/3E FPGA differential receiver input specifications. The simulation results are summarized in Table 2.

Table 2: **Summary of Figure 5 IBIS Simulation Results**

Parameter	Symbol	Typical
Simulated Differential output voltage	Vodiffsim	0.7V
Simulated Output common-mode voltage	Vocmsim	2.25V
Simulated Differential input voltage	Vidiffsim	0.5V
Simulated Input common-mode voltage	Vicmsim	1.5V

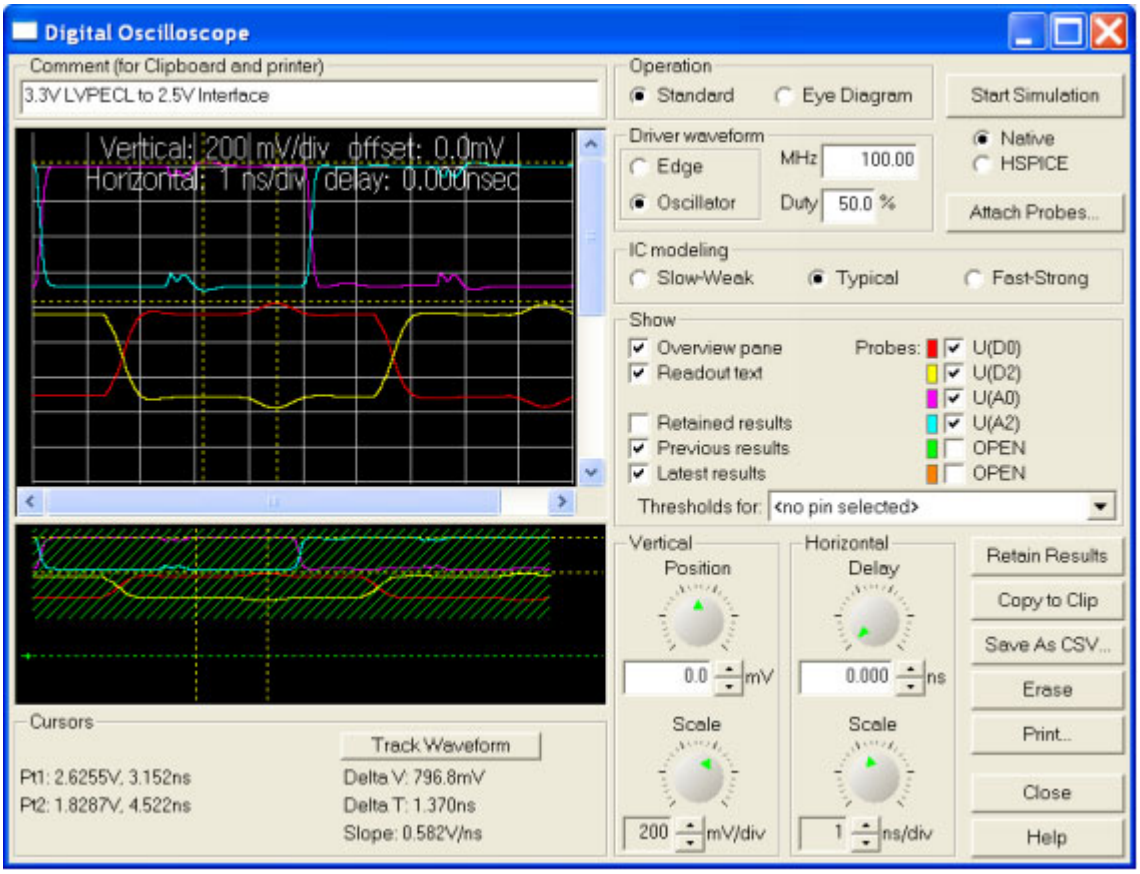

Figure 5: **3.3V LVPECL to 2.5V Receiver IBIS Simulation**

Note: The termination network shown in Figure 4 is intended for reference purposes only.

The optimal termination values are dependent on the driver output levels and could need to be adjusted to achieve optimal voltage levels at the receiver.

AC-Coupled Receiver Common Mode Voltage Shift

Inserting a series capacitor and biasing network into each leg of the differential receiver allows a reduction of the common mode voltage. This technique can provide protection against extreme DC voltages and can be useful for board-to-board or system-to-system interfaces. An example of such an interface is shown in Figure 6. AC coupling of links that have long idle periods, or where the signal is not DC balanced (the number of 1s and 0s average over time is not equal) might not be suitable. Also, the low frequency cut-off point of the high-pass filter formed by the series capacitor and receiver termination must be significantly lower than the minimum spectral frequency content, or data loss can occur. The component values shown in Figure 6 are suitable in applications where the minimum significant spectral content is about 1 MHz.

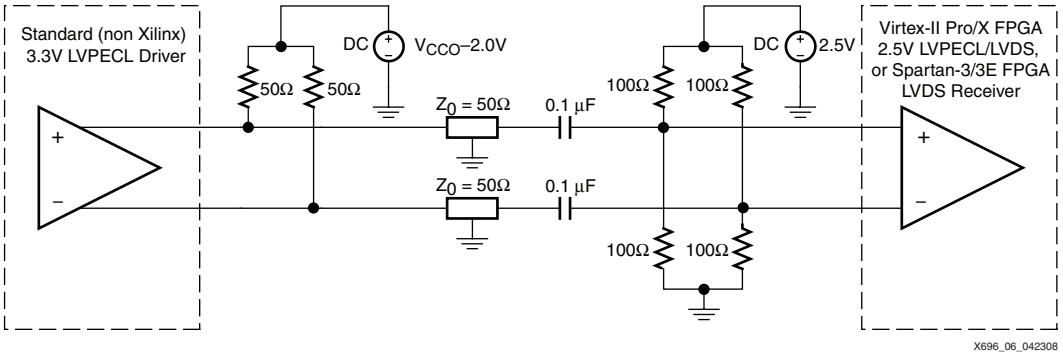

Figure 6: **3.3V LVPECL to 2.5V Differential Receiver AC-Coupled Interface**

Driver V_{CCO} Reduction

The common mode output voltage can be reduced to a low enough level by reducing the driver V_{CCO} value. This option can be evaluated by running an IBIS or SPICE simulation, or by bench testing.

Conclusion

Virtex-II Pro and Spartan-3/3E FPGA differential receivers typically cannot directly receive LVPECL 3.3V levels using standard 100Ωparallel receiver termination. However, by utilizing custom AC or DC-coupled termination schemes, such an interface can be effectively implemented. The LVPECL driver output voltage device specification should always be considered, and IBIS or SPICE simulation should be performed to determine the optimal interface termination scheme.

Revision History

The following table shows the revision history of this document.

Date	Version	Revision
05/21/04	1.0	Initial Xilinx release.
03/07/05	1.1	Typographical edit. Updated Figure 3 and Figure 4.
01/25/08	1.2	Added references to Virtex-4, Virtex-5, and Spartan-3E FPGA families.
05/1/08	1.3	Updated Figure 4.

Notice of Disclaimer