# AsAd Test bench

## ADS6422 test report

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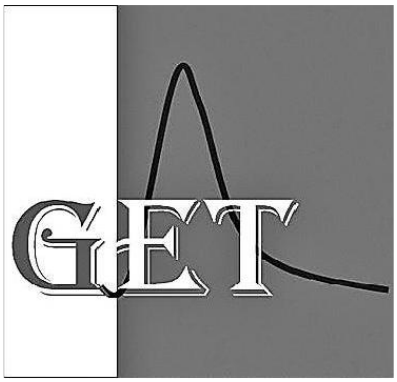


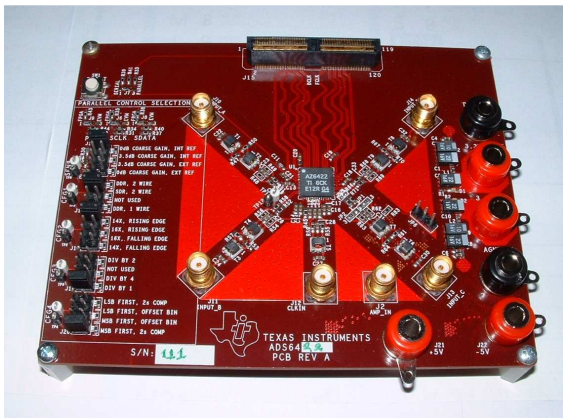

# Test Report ADC ADS6422

## Abstract:

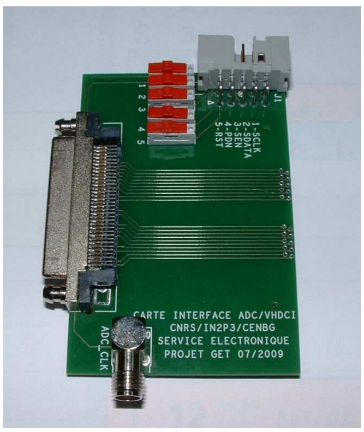
This document presents the specifications of the analog to digital converter ADS6422 from Texas Instrument.

## Materials:

- ADS6422EVM (evaluation board of ADS6422) [pic.1]
- ADS6422EVM ⇔ VHDCI interface [pic.2]
- VHDCI cable (1.80m and 3m length) [pic.3]
  Digi-Key part number: S456-006-ND for 1.80m and S457-010-ND for 3m
- VHDCI ⇔ LVDS buffer interface [pic.4]

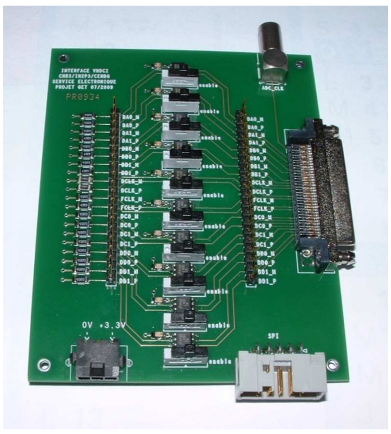



pic.1




pic.2

pic.3

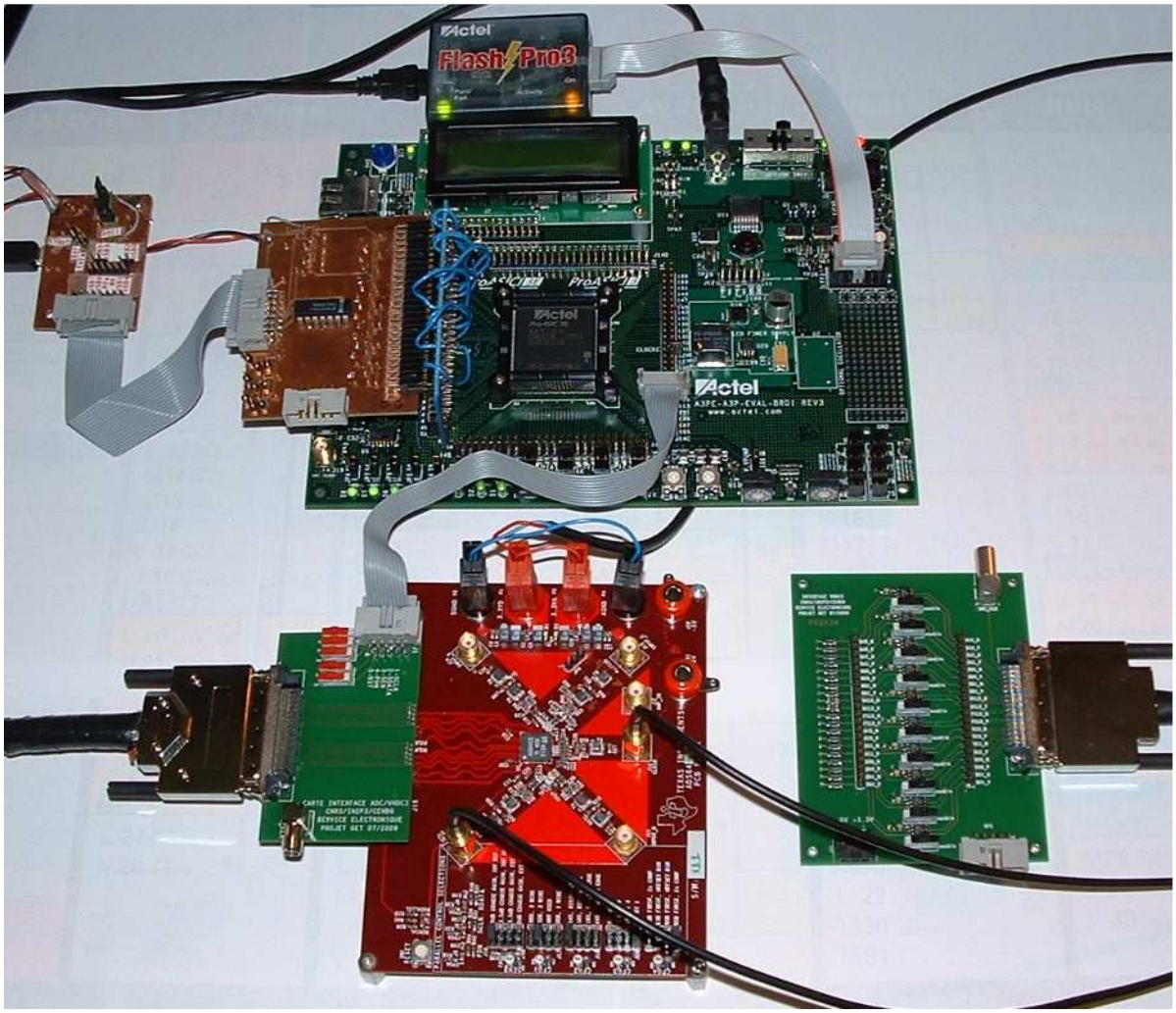


pic.4

## Test bench:

The test bench is composed of the evaluation board ADS6422EVM which include an output connector (Samtec QTH-60-02-F-D-A). Digital outputs and SPI protocol are available on this connector. The ADS6422EVM ⇔ VHDCI interface permits to connect the VHDCI cable to the evaluation board and HE10 connector to program the ADS6422 through SPI. At the end of the cable, there is a VHDCI ⇔ LVDS buffer interface to emulate the CoBo card. The buffers are National Semiconductor DS90LV001.

SPI protocol is generating by an FPGA PROASIC3E from ACTEL.




Test bench

## Set up:

The programming parameters of the ADS6422 are:

Register 00:
- all channels powered up
- internal reference

Register 04:
- default input clock buffer gain 1

Register 0A:
- output custom pattern
- data format 2s complement

Register 0B:
- D10=1 D9=0 D8=1 D7=0 D6=1 D5=0 D4=1 D3=0 D2=1 D1=0 D0=1

Register 0C:
- D11=0
- Fine gain control = 0dB

Register 0D:
- 2 wire interface
- SDR bit clock
- x12 serialization
- Capture at rising edge of bit clock
- 0dB coarse gain
- MSB first
- Byte wise
- Over-ride disable

Register 10:
- nominal LVDS current
- output current set to 2.5mA
- 100Ω LVDS internal termination for clock

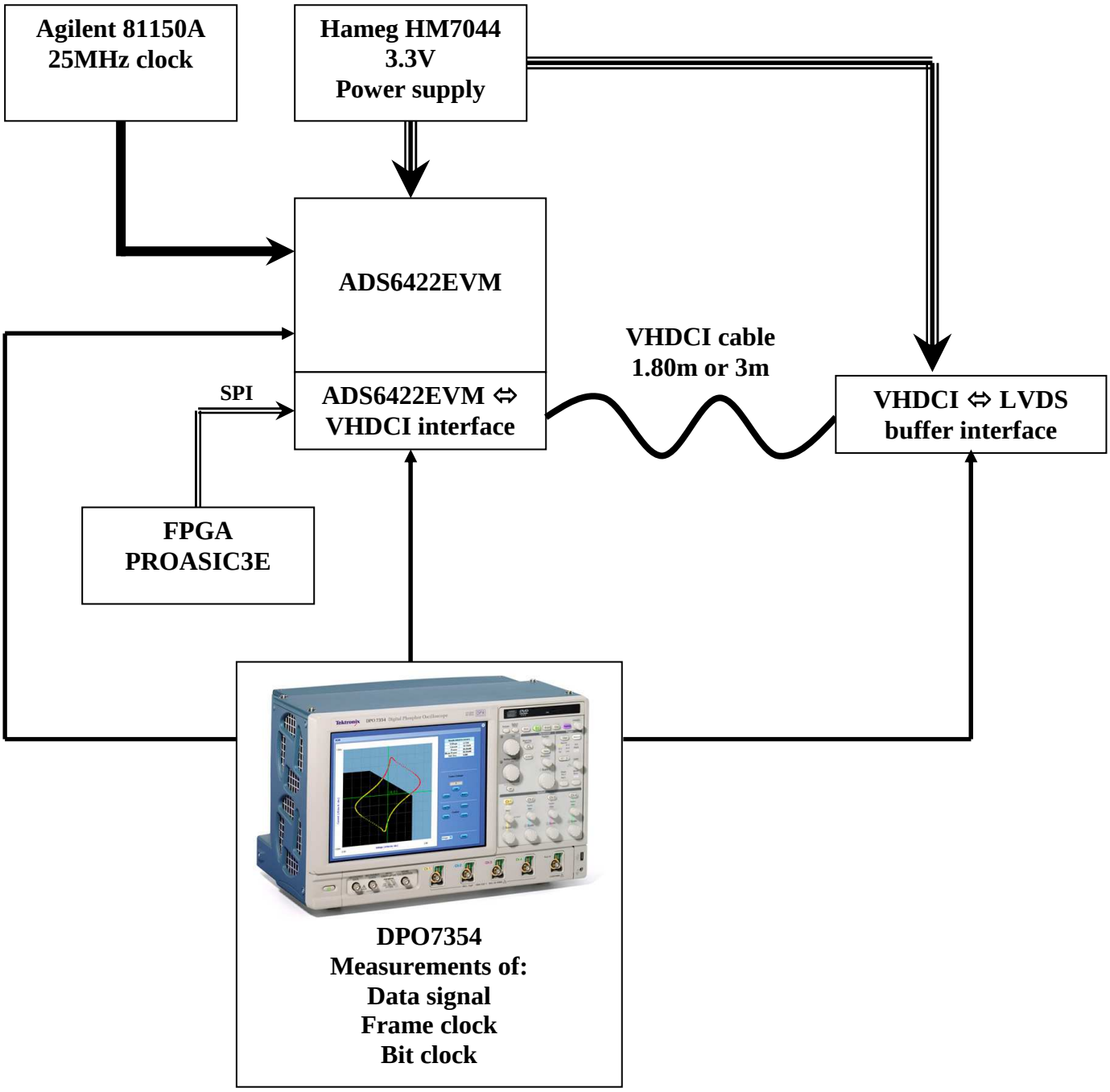
Register 11:
- 100Ω LVDS internal termination for data
- 1x frame clock

This data are programming with the FPGA PROASIC3E and send to the ADS6422 trough the HE10 connector of the ADS6422EVM ⇔ VHDCI interface. The protocol used is SPI.

## ADS6422 measurements:

Requirements:

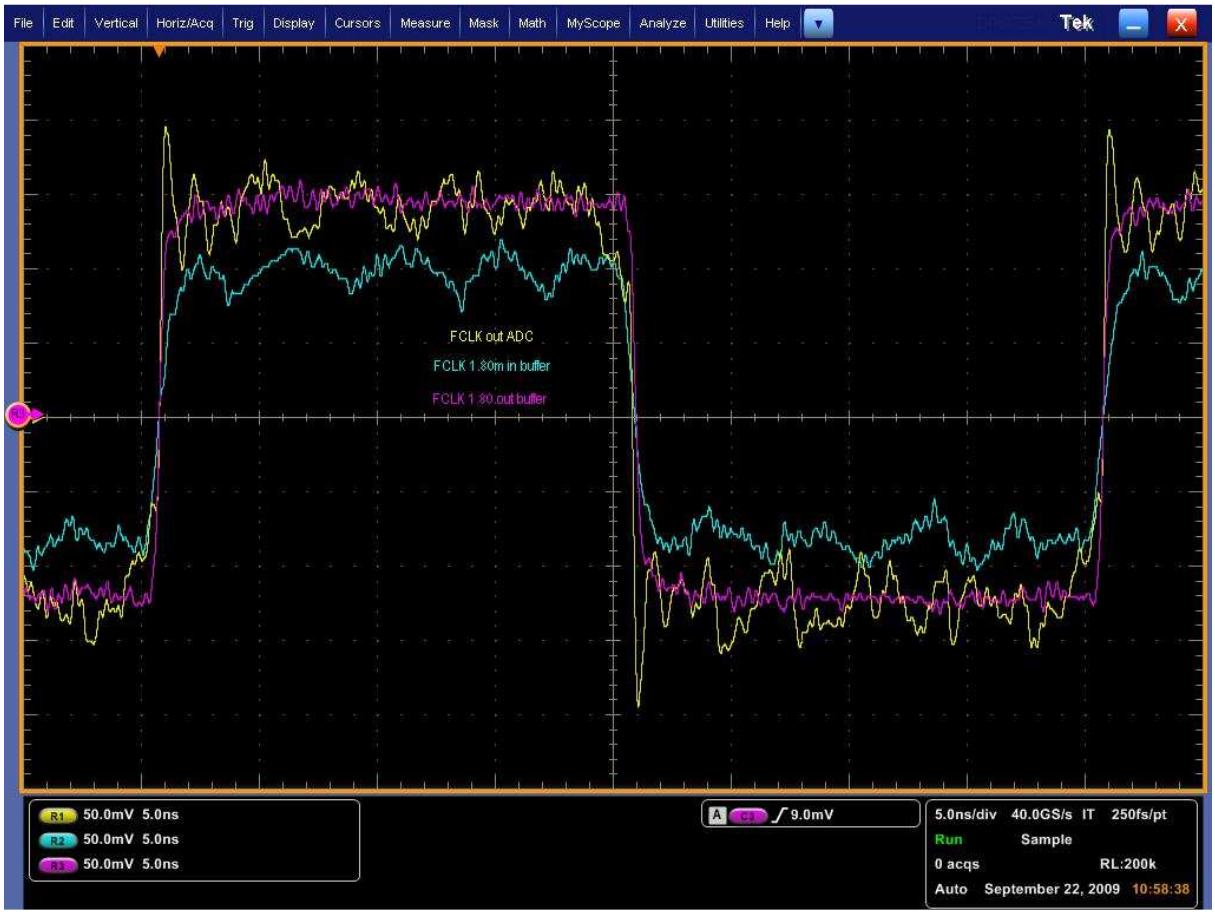
- Tektronix DPO 7354 3.5GHz digital phosphor oscilloscope
- Tektronix TDP3500 3.5GHz  differential probe
- Tektronix TDP1000 1GHz  differential probe
- Agilent 81150A pulse function arbitrary generator
- Hameg HM7044 power supply



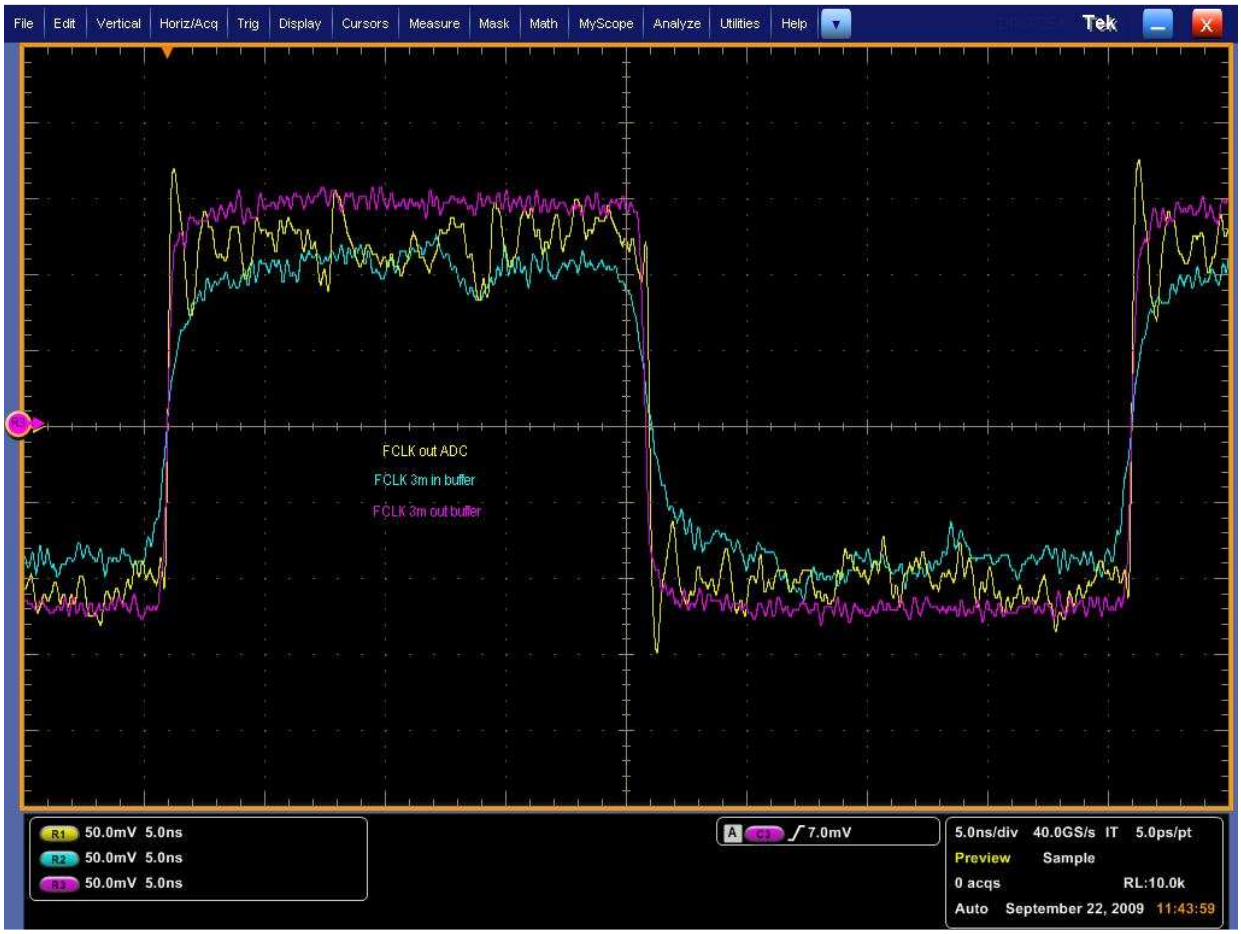
For the measurement, the clock of the ADC is set to 25MHz, which means that the output frequency of the frame clock is 25MHz and the frequency of the output bit clock is 150MHz. The measurements are made with 1.80m cable and 3m cable.

· Yellow curve is the direct differential output of the ADC (internal 100Ω termination)
· Blue curve is at the end of the cable at the input of the LVDS buffer with 100Ω differential termination
· Pink curve is at the direct output of the LVDS buffer with 50Ω load to ground on each way

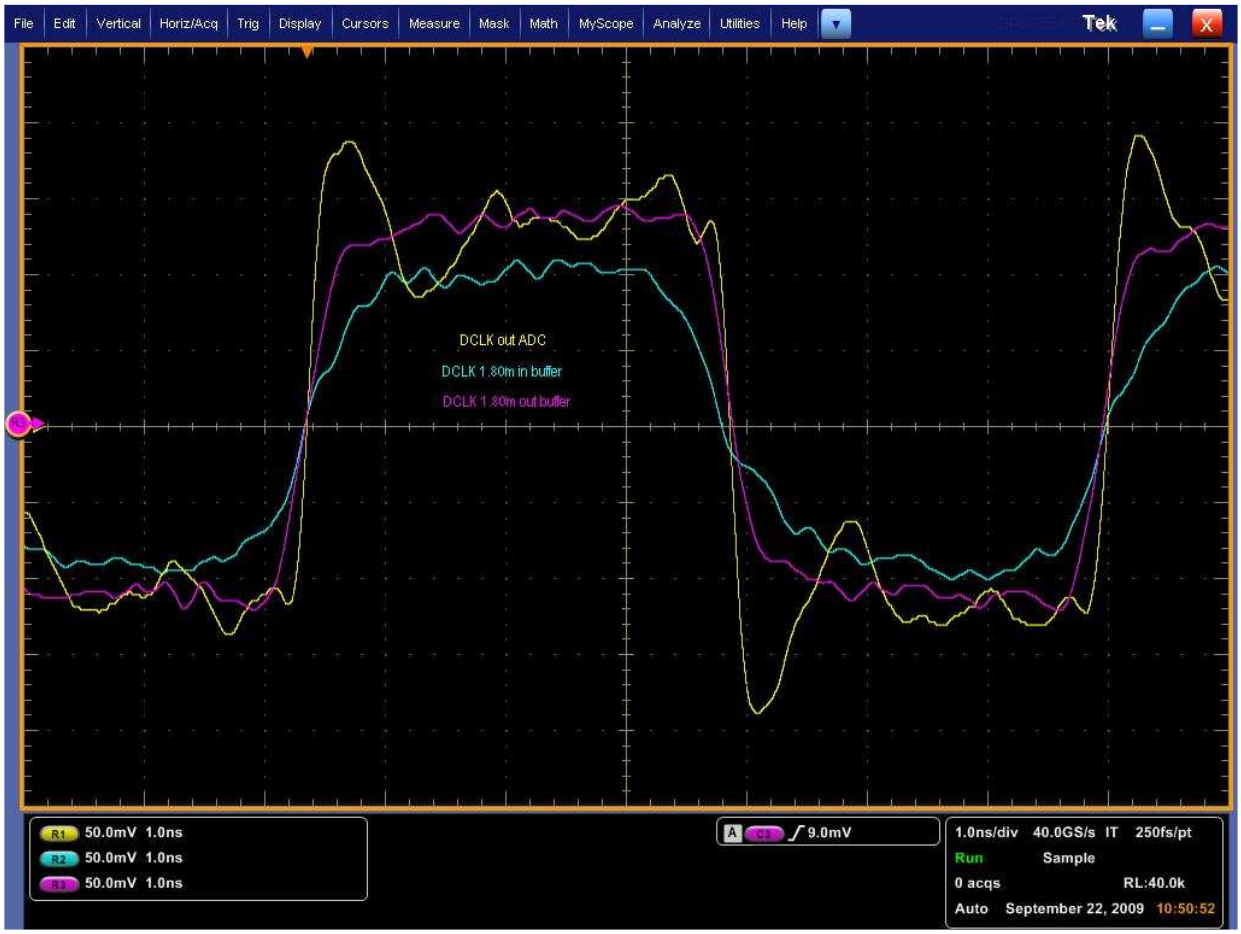
- Frame clock for 1.80m cable:



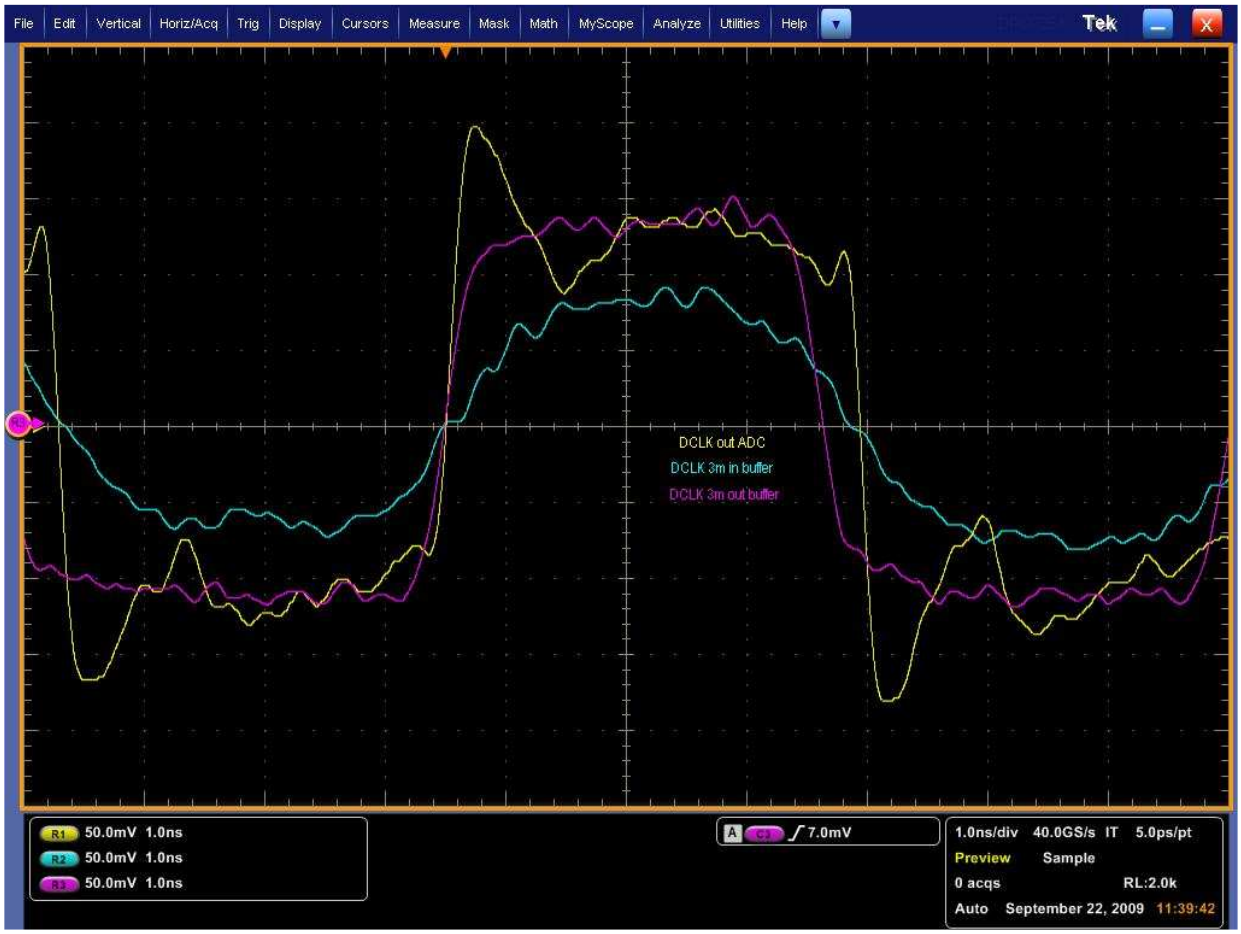
- Frame clock for 3m cable:



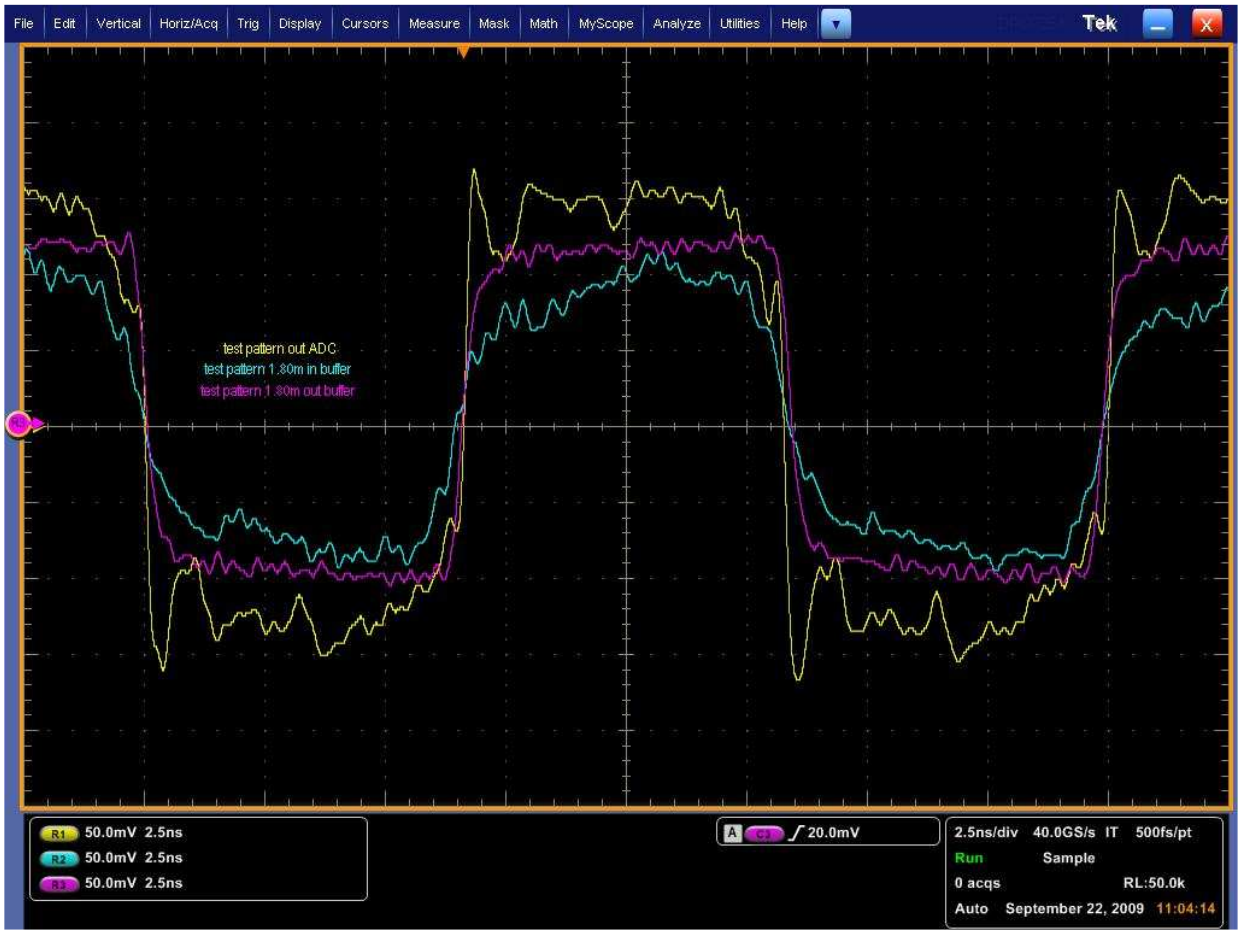
- Bit clock for 1.80m cable:



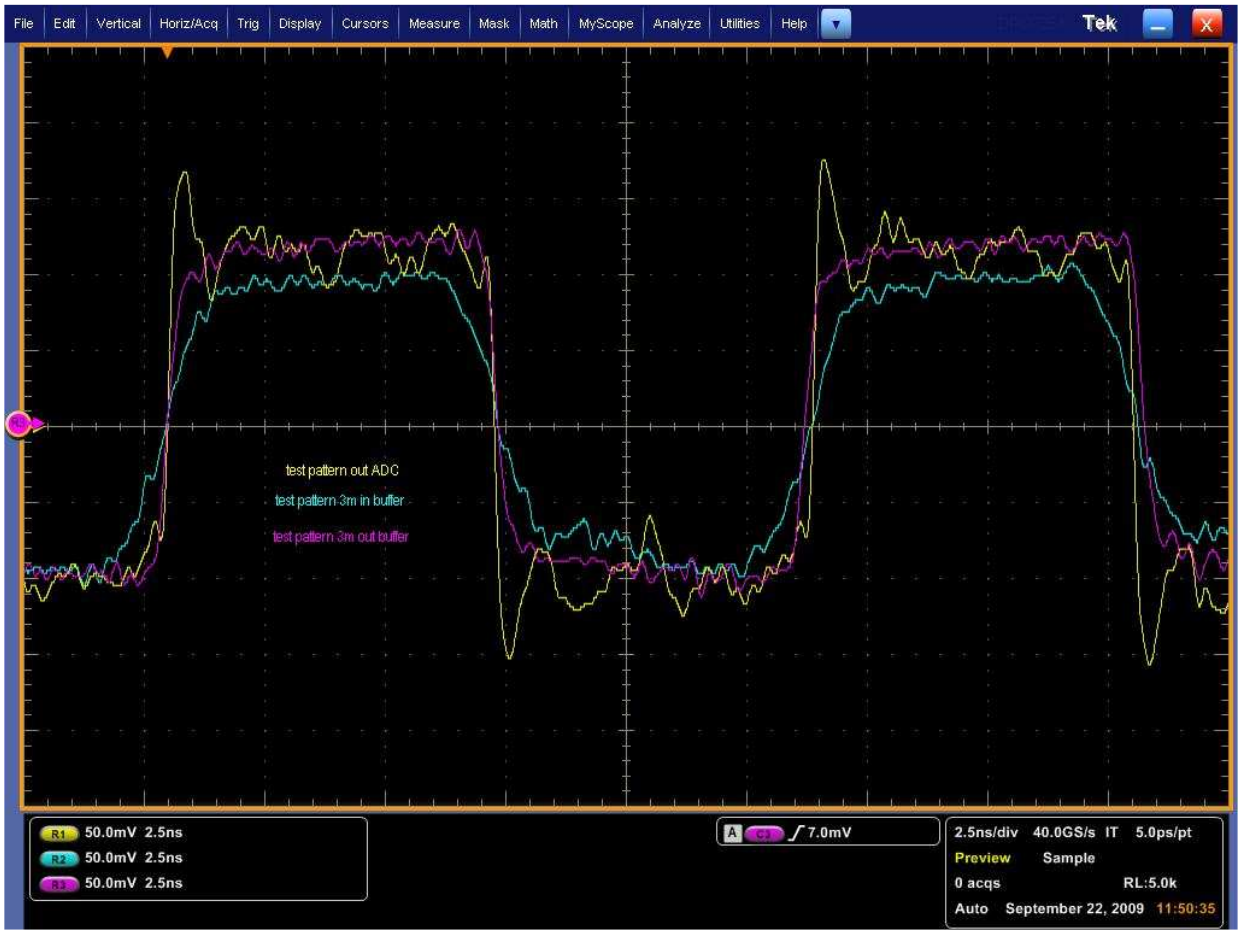
- Bit clock for 3m cable:



- Data test pattern for 1.80m cable:

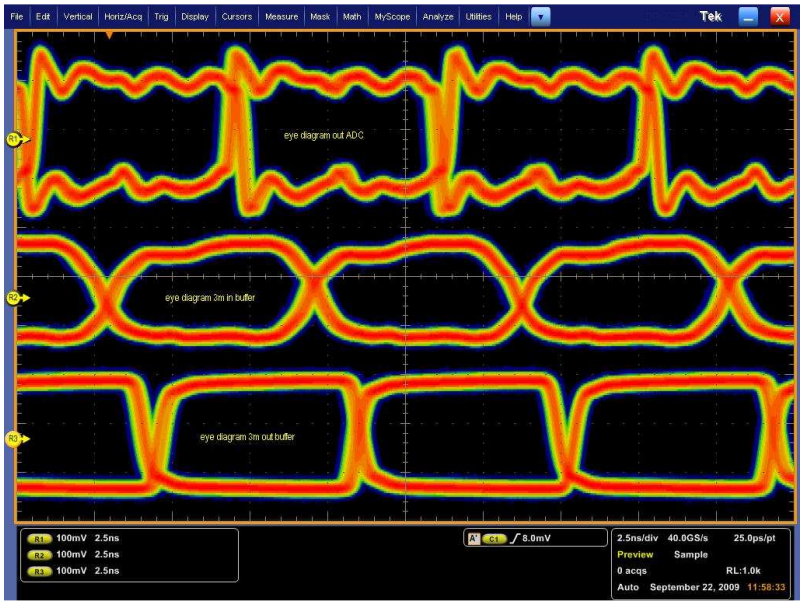


- Data test pattern for 3m cable:

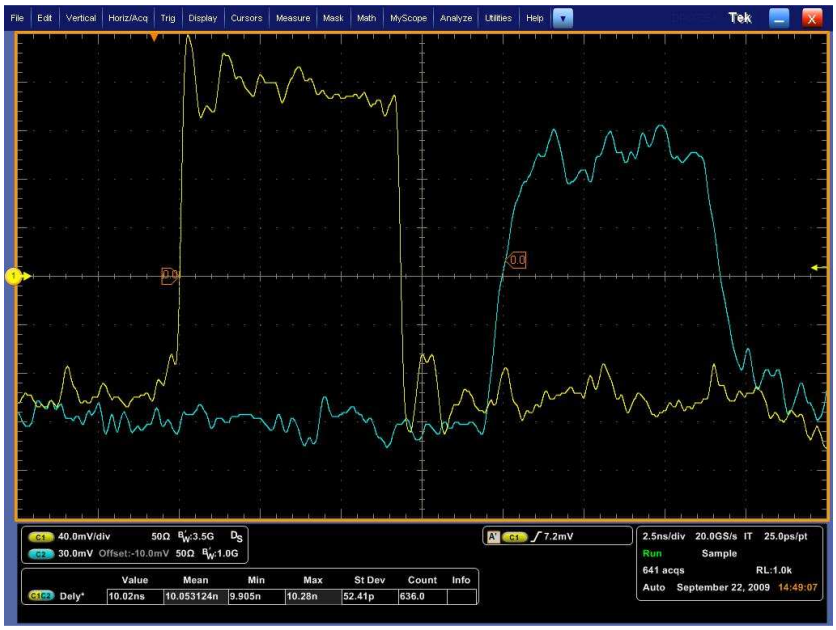


- eye diagram for 1.80m cable:

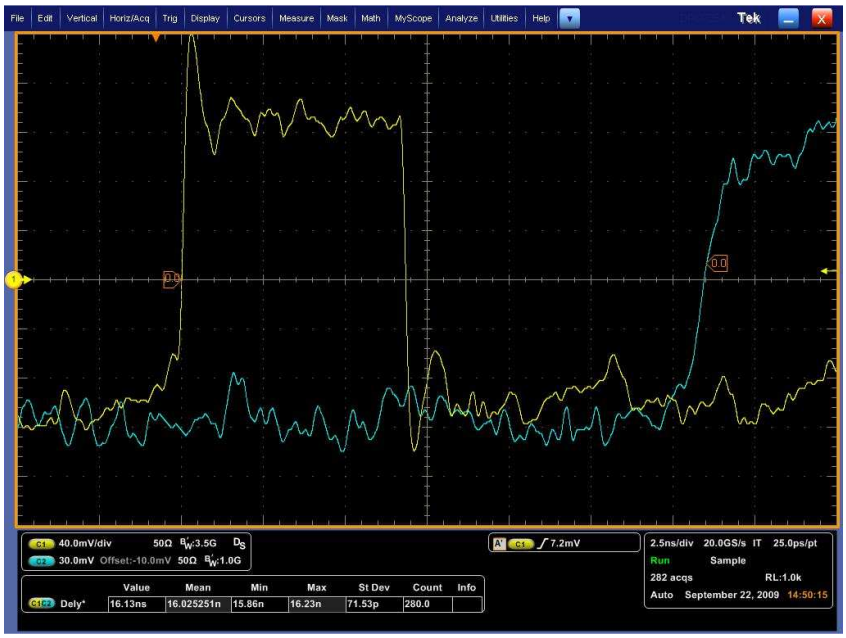

- Eye diagram for 3m cable:



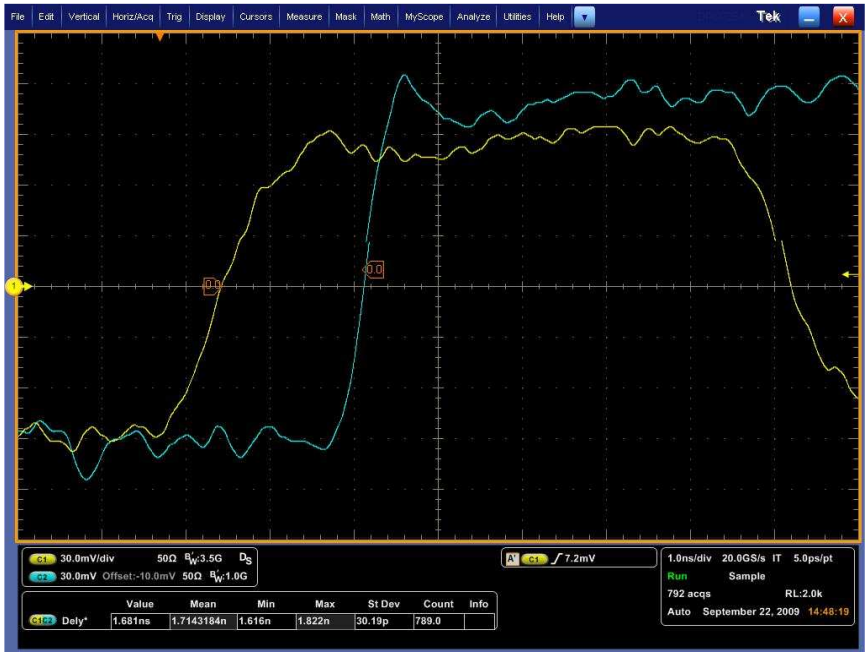
- delay of data signal between ADC output and end of 1.80m cable: <u>10ns</u>




- delay of data signal between ADC output and end of 3m cable: <u>16ns</u>

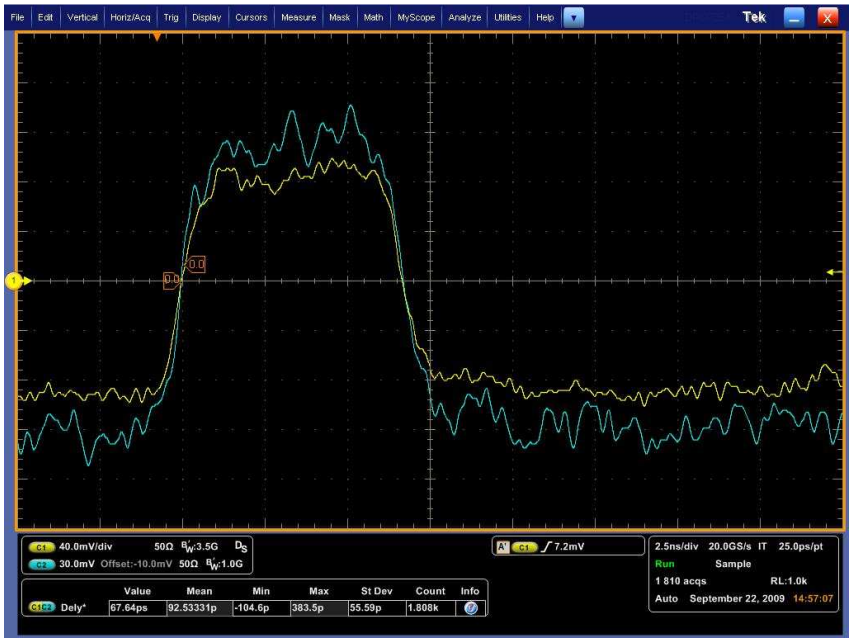


- delay of the LVDS buffer: 1.6ns

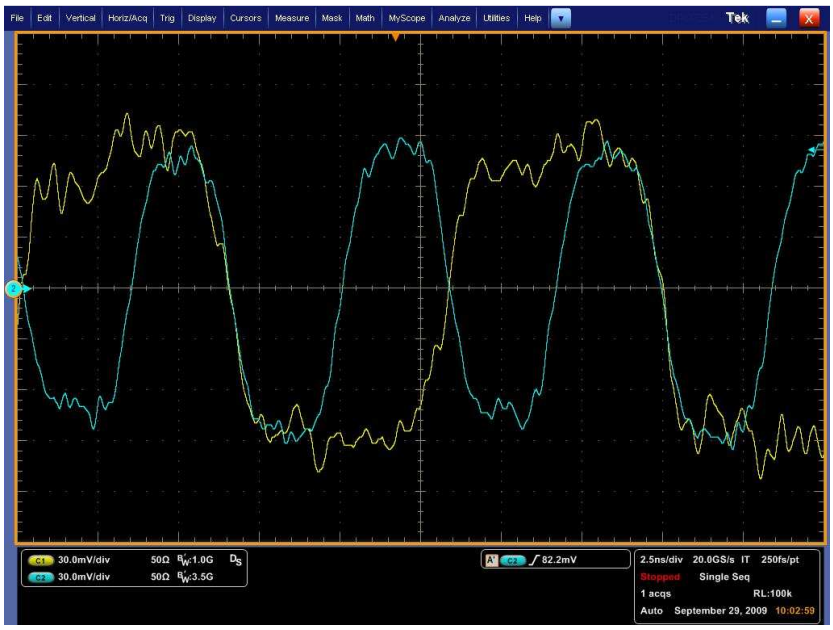



- delay between two data output: null

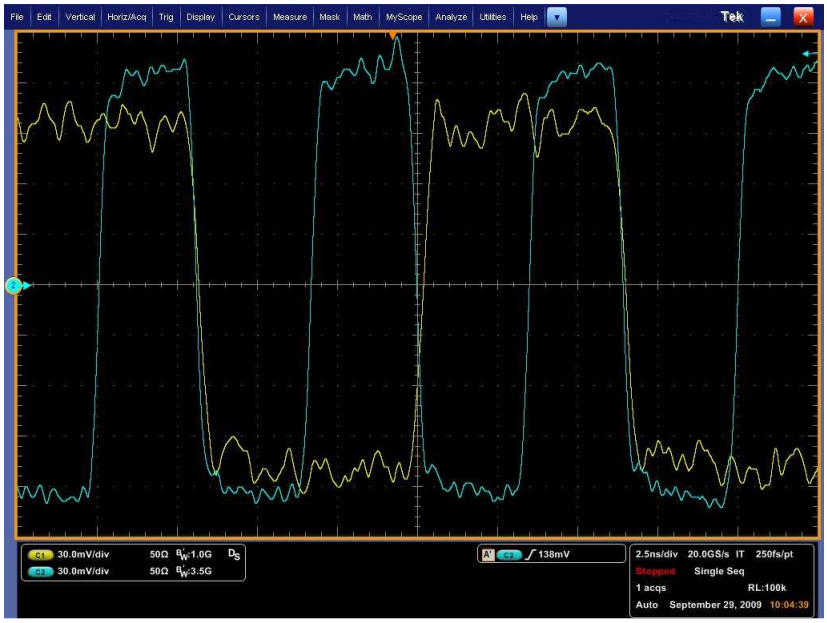
I used two differentials probe, a DP3500 and a DP1000. The delay between the two probes is 800ps which is compensated by deskew on the oscilloscope. The delay is near 0.



- Signal DA0 and bit clock at the end of 3m cable:




- Signal DA0 and bit clock at the end of 3m cable after buffer:



- Signal DA0 and frame clock at the end of 3m cable: