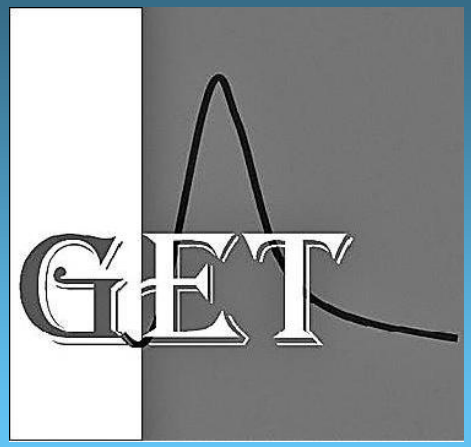

Technical constraints & strategy

μelectronics : AGET

- Finalize AGET « particularities »
  - The goal is to have a submission for next July
    - Fix the chan number (even modification the packaging will be the same FEC test bench)
    - Special usage of the ring buffer for 2p radioactivity

    . Fix fast mode pattern readout (50 MHz ?)

    - ….

Electronics

- Finalize all specifications
  - From draft to V1.0 version
  - Feedback from the revue team
- Fix physical connections between subsystems
- Fix ZAP location (if required) AND therefore connection between E.M. and FE.
- Decide of the max length between CoBo & AsAd
- Fix logical connections between subsystems (ie slow control « generic protocol »)
- Decide necessary data rate out of CoBo
  - 10 Gb Ethernet, 1 Gb Ethernet, 2x 1 Gb Ethernet

Need to

- Increase communication frequency between designers
- Begin a real simulation or/and test protocol for fuzzy points :
  - Connectors and cables
  - Bufferize ADC output
  - Pulser-Calibration functionalities
  - MUTANT master clock distribution