



**MU**ltiplicity **T**ime **AN**d **T**rigger  
Module

**Specifications**  
*Draft 0.1*

Overview .....	2
Chapter 1: Specifications .....	4
1.1 Characteristics and functions .....	4
1.1.1 Standard.....	4
1.1.2 System size .....	4
1.1.3 Clock tree .....	5
1.1.4 Level Ø trigger .....	6
1.1.5 Level 1 trigger .....	6
1.1.6 Level 2 trigger .....	7
1.1.7 Event Number .....	7
1.1.7 Time Stamp .....	7
1.1.8 Global Reset/Synchronisation Method.....	7
1.2 Front panel links.....	8
1.2.1 to CoBo's.....	8
1.2.2 to slave MUTANT .....	9
1.3 Coupling with Back End Module (BEM) .....	9
1.4 Visualization.....	9
Chapter 2 : I/O Signals .....	10
2.1 Front panel inputs.....	10
2.2 Front panel outputs.....	12
Chapter 3 : The MUTANT registers .....	14
3.1 General configuration register (Slow control) .....	14
3.2 Inspection and diagnostic Registers .....	14
3.3 Data readout Registers .....	14
Appendix 1: NIM architecture .....	15

## Overview

The aim is to design and build the electronic device that, within GET, will manage the multiplicity, the conditions for the trigger, the distribution of a clock on the whole system for synchronisation and the time stamp information for every sub event.

A particular attention to these aspects is due in a system destined to be coupled to the new generation nuclear physics detectors. At 20000 channels or more, the traditional techniques of Trigger used in nuclear physics (analysis-windows + sequencer) are not sufficient any more today in terms of functionality and of integration.

The device is named: MUTANT for MULTiplicity Trigger ANd Time.

The reason for developing this type of module, for the GET data acquisition, is to have a custom electronic that support multiple TPC detectors. The main features or requests for this board are:

- NIM mechanical and electrical standard, double unit
- Scalable system with no extra board to design
- Providing a clock tree where the root oscillator is the internal clock of MUTANT or an external reference clock
- Global reset/synchronisation method
- Level 0 trigger called “external trigger”
- Level 1 trigger called “multiplicity trigger”
- Level 2 trigger called “trigger on bit pattern”
- Distribution of an event number ( useful in common dead time)
- Distribution of time stamp values
- Fully programmable (by slow control) or readable during acquisition, all that by Ethernet network (TCP/IP)
- Easy to integrate in existing data acquisition system with CENTRUM @ GANIL, BUTIS @ GSI or in an other DAQ via the Back End Module (BEM)
- Able to work in common dead time mode or in autonomous mode

Here is a very preliminary version of the specifications for MUTANT. This list is not exhaustive, and every item is described in more details in the next chapters. Central to both discussions is a synchronisation method allowing all the channels to work in phase and when

there is a valid event, after a combination of L0, L1 and L3 triggers, a piece of information is sent and added to the sub event buffer (in each CoBo). All sub events are then forwarded to the PC's. The time information will be used later in the event builder to merge data from the different apparatuses (CoBo modules), all that to build the global event.

In essence the proposal is, as CoBo, for a NIM sized module. The parallel bus is no more necessary today in such application where every module is equipped with CPU(s) plus embedded operating system (LINUX) and is able to talk directly over the network with high speed serial protocols. But cooling and good power supplies stay a very important point which is appreciable to find on the shelf with high power NIM crates and not to have to waste time to design or assembly them.

## Chapter 1: Specifications

### 1.1 Characteristics and functions

An idea of the NIM architecture is given in appendixes 1.

#### 1.1.1 Standard

This instrumentation module is designed in conformance to NIM standards. It will be, at the hardware point of view, the same module in every crate (MUTANT type, id. code 0x3).

[http://groups.nsl.msu.edu/tpc/wiki/lib/exe/fetch.php?id=electronics&cache=cache&media=get\\_board\\_id.pdf](http://groups.nsl.msu.edu/tpc/wiki/lib/exe/fetch.php?id=electronics&cache=cache&media=get_board_id.pdf)

The full system can be seen as a starry daisy-chain. The option for MUTANT, master or slave, will be defined only by software (slow control setup). The whole system could be considered as a master MUTANT that will be the maestro of the TPC DAQ exchanging data with other NIM crate via slave MUTANT that will act typically as “intelligent FAN IN/FAN OUT”. As the width of a NIM crate is twelve slots and a MUTANT occupies 2, the MUTANT controls maximum ten CoBo modules in its own crate (i.e. 11520 channels).

#### 1.1.2 System size

The system must scalable up to 20 000 channels but an upper bound must be defined, for the architecture, to clearly identify the constraints in terms of propagation delay, pipeline of the system and global synchronisation method. As mentioned previously, the maximum is 288 ch /ASAD, 1152 ch / CoBo and finally 11520 channels per NIM crate. The digital multiplicity coming from a CoBo to MUTANT will be received every 40ns (25 MHz sampling rate). This one will be coded on 11 bits and 14 bits will be necessary to regroup the multiplicity at the crate level.

The proposal is to control the whole multiplicity of a TPC on sixteen bits, fifteen significant bits plus one parity bit to rapidly identify decorrelation between crates. That lets up to 32767 channels with 1152 channels by CoBo, so it's about 28 (fully used) to 30 (maximum) CoBo's in three crates for the largest GET system. I also propose to add a twelfth bit for the multiplicity value coming from each CoBo to also check the parity at the CoBo level.

### 1.1.3 Clock tree

One master clock signal must be distributed to the whole system, from master MUTANT to ASADs via CoBo's if in the same chassis or via slave MUTANT if in an other crate. This, essentially to have only one clock domain for the "WRITE SCA" clock of every AGET and to stay fully synchronised along the chain especially to build the numerical multiplicity from the ADC of each ASAD to the master MUTANT. The distribution of a master clock signal of 100 MHz seems enough to cover the different required configurations or the necessary divided frequency. Dividers circuits with skew correction and jitter limitation can be locally implemented on boards. The next table summarizes all the options:

F write_sca (MHz)	Corresponding Tdrift (511 cells)	Corresponding Tdrift (256 cells)
100	5,11 $\mu$ s	2,56 $\mu$ s
50	10,22 $\mu$ s	5,11 $\mu$ s
25	20,44 $\mu$ s	10,22 $\mu$ s
<i>12,5</i>	<i>40,88 <math>\mu</math>s</i>	<i>20,44 <math>\mu</math>s</i>
<i>6,25</i>	<i>82 <math>\mu</math>s</i>	<i>40,88 <math>\mu</math>s</i>
<i>3,125</i>	<i>164 <math>\mu</math>s</i>	<i>82 <math>\mu</math>s</i>
<i>1,5625</i>	<i>328 <math>\mu</math>s</i>	<i>164 <math>\mu</math>s</i>

As the electronic is general (GET) and the AGET circuit has been designed to work from 1 to 100 MHz, it is useful for the design of all the boards to use a factor two of division starting from the highest frequency (100 MHz) to the lowest (1,5625 MHz). The lower frequencies values (in italic) may not need to be implemented on boards if such associated drift times are not physics cases with TPC's. As these frequencies have to be selectable by slow control, if intermediates frequencies are required (i.e. 40 MHz) it must be mentioned for the design of boards. Even if the MUTANT module is equipped with an internal good quality oscillator (typically 200 MHz/few ppm), the module will have "LOCAL\_CLOCK\_IN", "LOCAL\_CLOCK\_OUT" all that differential to be inter-connectable between MUTANT (Master/Slave) and a "REMOTE\_CLOCK\_IN" from BEM (optical fibber) to be easily connectable to other clock source of other systems.

### 1.1.4 Level Ø trigger

The MUTANT module will have a LØ (External trigger) input to make a coincidence with an other detector (beam tracker, silicon detector...) and a L1 (multiplicity) trigger from the TPC. We can imagine having the choice by slow control that one (LØ or L1) start a programmable window of MUTANT (width & resolution to be defined...) waiting for the coincidence with the other one (LØ or L1). This input will be local (front panel) or remote (from BEM) via optical fiber. The other option is to imagine the TPC as an ancillary detector of a master trigger with a couple of Trigger Request/Trigger validation (local or remote).

### 1.1.5 Level 1 trigger

After discussions, the choice of digital multiplicity has been adopted. The multiplicity signal use the same path as the analog samples at the ASAD level and are both digitized at 25 MHz before reaching the CoBo level. The role of MUTANT in this scenario is first to get the partial multiplicity from all the CoBo's used in the acquisition and to build the total multiplicity. This must be done in a sliding time window depending of the "WRITE\_SCA\_CLOCK" frequency ( $\approx 5\mu\text{s}$  @ 100MHz,  $10\mu\text{s}$  @ 50MHz ... for 511 cells). Secondly, after the choice of a threshold that has been programmed by slow control before starting the acquisition, the internal logic examine if the sum is equal (or superior) to this value and give the signal "L1\_TRIGGER\_OK" in case of success. Even if there is an extra level of analysis (L3), the MUTANT must send the "STOP\_WRITE\_SCA" as fast as possible. The rule for MUTANT is to follow the sampling rate of the multiplicity (every 40 ns) and to take a decision at the end of a few cycles pipeline (based on the master clock). So, the proposal here is to collect multiplicity from CoBo by nibbles (4 bits), three cycles will be necessary to have the full multiplicity of every CoBo as input of every MUTANT (all that in parallel). After that the master MUTANT will receive the multiplicity from the one or two slave MUTANT by, inter crates, daisy-chain cables. This can be done in less than 100 ns. In case of positive decision from L1 trigger, two possibilities:

- There is no L3 trigger programmed and after the "STOP\_WRITE\_SCA" received by the CoBo's, in response a "DEAD\_TIME" signal is issued by everyone until they have finished treating the current sub event. The "STOP\_WRITE\_SCA" signal will be released only after a zero result from an "OR" function of all the "DEAD\_TIME" (in common dead time mode). The asserted "STOP\_WRITE\_SCA" acts also as an inhibit for the CoBo's that are ready to restart. Following that, MUTANT waits for a new valid event (multiplicity threshold) and so on ...

- There is a L3 trigger programmed and after crossing the threshold starts a complementary phase. See next chapter.

### **1.1.6 Level 2 trigger**

After a “STOP\_WRITE\_SCA” signal, the master MUTANT gets a picture of all the TPC pads via the CoBo’s by reading the bit pattern of every AGET. This information stored in the FPGA memory could be analysed by preloaded memory fast comparison or embedded algorithms processed by the FPGA PowerPC. If the event is rejected, the “STOP\_WRITE\_SCA” is negated synchronously and the system could restart. If the event seems interesting, all the fired channels can be digitized directly or a mask applied on the readout pattern can be written back to the AGET’s to only convert the right channels.

### **1.1.7 Event Number**

A 32 bit loadable counter will be incremented on every accepted event after a positive decision of the selected trigger combination (L0, L1 and/or L2). The current 32 bit value, accompanying the time stamp value, will be broadcast by the master MUTANT to all the CoBo’s being in common dead time. If, in a second step, an autonomous mode is used, “free running CoBo”, this feature will be automatically disabled.

### **1.1.7 Time Stamp**

A universal time counter (clocked by the master clock, i.e. 100 MHz) with a preload register, 48 bits wide to cover one month of experiment, is also included in the module. This one will begin to increment on the “START ACQUISITION” command. As the requirement here is time stamping and not TDC function, the use of 10 ns resolution satisfies the condition of sub event identification by absolute clock tagging. The idea is to distribute the full information from the core of MUTANT and not to have local counters that need to be regularly resynchronized. If in the future, an autonomous mode is used, every CoBo will have their own tagging and readout register.

### **1.1.8 Global Reset/Synchronisation Method**

As explained at the beginning of this document, it is important to have the system totally in phase with respect to the master clock signal of 100 MHz. For that we can imagine a



reset/sync pulse emitted from an output of the master MUTANT and buffered by a commercial NIM FAN OUT module. All the outputs of this one send the same signal with the same cable length to an input of each CoBo, resetting/starting their internal clock generator (Phase Matched Clock Divider, PMCD by Xilinx). Every MUTANT analyses the incoming multiplicity frame signals delivered by the CoBo's and knows if they are in time. After that correction can be applied at the CoBo or Mutant level. In a second step, training patterns can be sent from CoBo to check the link CoBo-Mutant to be sure that the multiplicity bus is sampled at the right time with the right values.

## **1.2 Front panel links**

Here is described, at the connection point of view, how MUTANT communicates with the CoBo's and other MUTANT, depending if it is master or slave.

### **1.2.1 to CoBo's**

The PCB connectors used are stacked 2x15 points MDSM connectors from ITT-Cannon (MDSM-30PE-Z10-VR22). They have good EMI shielding and are especially designed to save space on front panels. The cable used (shielded twisted pair) and the cable connectors are also supplied by ITT-Cannon or Molex. Each connector and cable carrying differential signals has 7 twisted pairs and a single ended one.

The first one is dedicated to the clock distribution and the reception of the current multiplicity. They are used as follows:

- MASTER\_CLK (out)
- MULT\_DATA<3..0> (in)
- MULT\_FRAME (in)
- STOP\_WRITE\_SCA (out)

The second one is mainly dedicated to serial information distribution. Even if the transmission frequency is lower (50 or 25 MHz) and the distances are short, it's safe to still use differential signals.. They are used as follows:

- DEAD\_TIME (in)
- SERIAL\_CLOCK (out)
- SERIAL\_FRAME (out)
- SERIAL\_DATA (out)

- ...

### **1.2.2 to slave MUTANT**

A stacked sixty four pin connector (differential) using IN/OUT ways establishes the link between MUTANT's (daisy-chain). A sixteen bit bus is used to carry the multiplicity or the fired channels (patterns) from the two slaves MUTANT to the master one. In the same cable, on the opposite way, two serial links are also dedicated to transmit the information (time stamp, event number or selected pattern to read). Commercial cables are available with a length of 2 or 3 meters. The transmission frequency with this type of link is guaranteed at 50 MHz.

### **1.3 Coupling with Back End Module (BEM)**

The idea of BEM is to use it when long distance interface is a fact or when coupling with other systems (with time stamping, master trigger ...) is required as MUTANT can't host all the I/O for the multiple systems used in the different laboratories. But MUTANT must have the essential internal functions to control the GET electronics, and may be one silicon detector or beam tracker in an experiment, when coupling with bigger acquisition system is not required. What must be defined here are the necessary signals that MUTANT has to manage to communicate with the external or remote world, for example:

- REMOTE\_CLOCK\_IN
- TRIGGER\_REQUEST
- TRIGGER\_VALIDATION
- LOGIC\_INSPECTION\_1
- LOGIC\_INSPECTION\_2
- ...

For this purpose an optical module will be implanted on the board (rear panel) to send or receive signals from distances up to 300 meters.

### **1.4 Visualization**

As in a such system there is potentially a lot of signals to examine for any reasons (test, calibration, broken link ...) The front panel NIM output signals "TEST1" and "TEST2" (LEMOØØ) are generic and programmable. They will be used to control the timing of the tagging inputs, to view other internal signals on a scope or to trigger other module's inputs.

## Chapter 2 : I/O Signals

Some of the main connectors are detailed below.

### 2.1 Front panel inputs

**LEMO 00:** NIM level (-800 mV on 50  $\Omega$ )

**TRIG\_VAL** TRIGGER VALidation

Description:

Input signal that could be used by a master trigger (level  $\emptyset$ ).

**SMA:** LVPECL (50  $\Omega$ )

**LOCAL\_CLOCK\_IN+**

**LOCAL\_CLOCK\_IN-**

Description:

External input for the master clock (from master for slave MUTANT) or from local external source if master MUTANT.

### *15 pins connectors :*

**C15\_IN** RX data

Description:

This fast serial input is used to get data from the CoBo's (Multiplicity).

Logic levels

Differential LVPECL.

***64 pins connectors :*****C64\_IN**      RX data*Description:*

This fast serial input is used to get multiplicity and bit pattern from slave MUTANT and to transmit information (EVT NUM,TS, pattern to read).

*Logic levels*

Differential LVPECL.

## 2.2 Front panel outputs

**LEMO 00 connector:** NIM level (-800 mV on 50  $\Omega$ )

**TRIG\_REQ** TRIGGER REQUEST

Description:

Output signal that could be received by a master trigger (level  $\emptyset$ ).

**DT** Dead Time

Description:

This signal indicates that the GET electronic is busy, treating an event.

**RST/SYNC** RESET/ SYNCHRONISATION

Description:

Output signal used for GET clock synchronisation.

**TEST1 and 2**

Description:

TEST1 and TEST2 are used to output some MUTANT internal signals for timing control, diagnostics or triggering other modules.

**XXX...**

Description:

...

**SMA:** LVPECL (50  $\Omega$ )

**LOCAL\_CLOCK\_OUT+**

**LOCAL\_CLOCK\_OUT-**

Description:

External output of the master clock (from master to slave MUTANT).

**15 pins connectors:**

**C15\_OUT** TX dataDescription:

This serial output will be used to send all type of information to the CoBo's.

Logic levels

Differential LVPECL.

**64 pins connectors :****C64\_OUT** RX dataDescription:

This fast serial output is used to send the multiplicity and bit pattern from slave MUTANT and to receive information (EVT NUM,TS, pattern to read).

Logic levels

Differential LVPECL.

## **Chapter 3 : The MUTANT registers**

### **3.1 General configuration register (Slow control)**

*To be defined*

### **3.2 Inspection and diagnostic Registers**

*To be defined ...*

### **3.3 Data readout Registers**

*To be defined ...*

**Appendix 1: NIM architecture**

