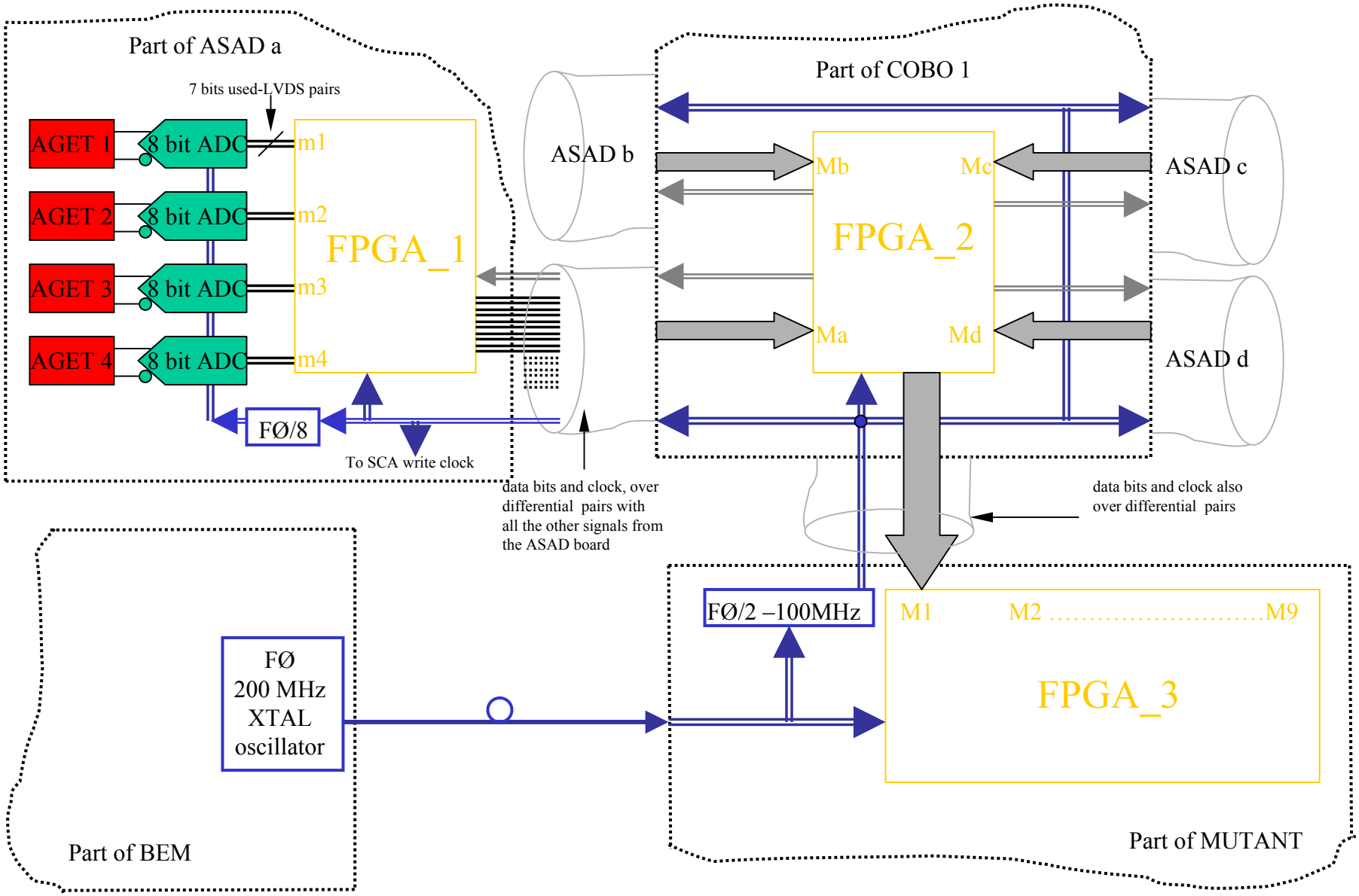
How to build the multiplicity (Version 2)



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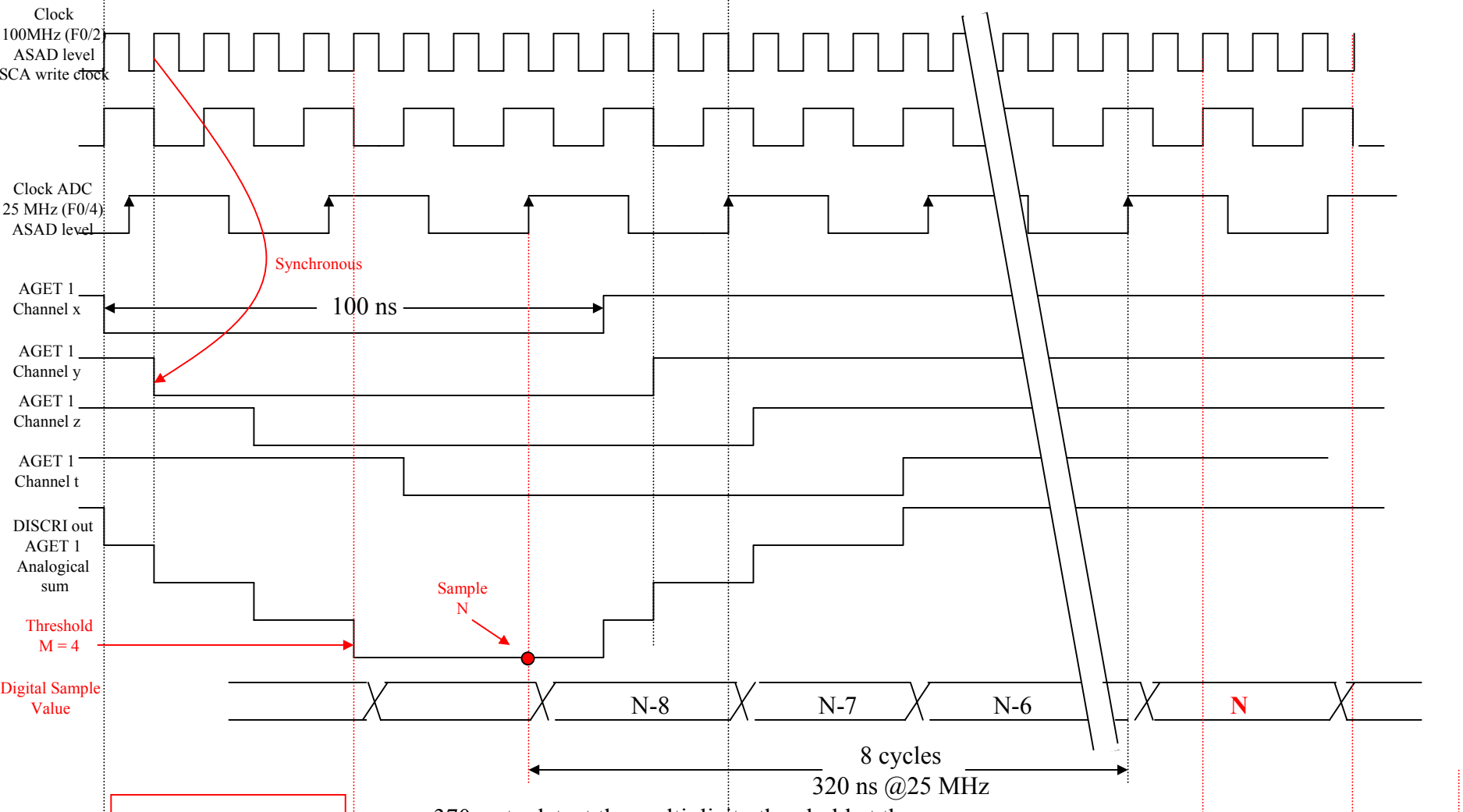
Multiplicity timing details



Worst case estimation using 8 bits pipelined ADC @ 25 MHz

≈370 ns to detect the multiplicity threshold at the AGET/ASAD level and open the coincidence window

≈ 400 ns to detect the multiplicity threshold at the COBO level and open the coincidence window

≈ 500 ns to detect the multiplicity threshold at the MUTANT level and open the coincidence window

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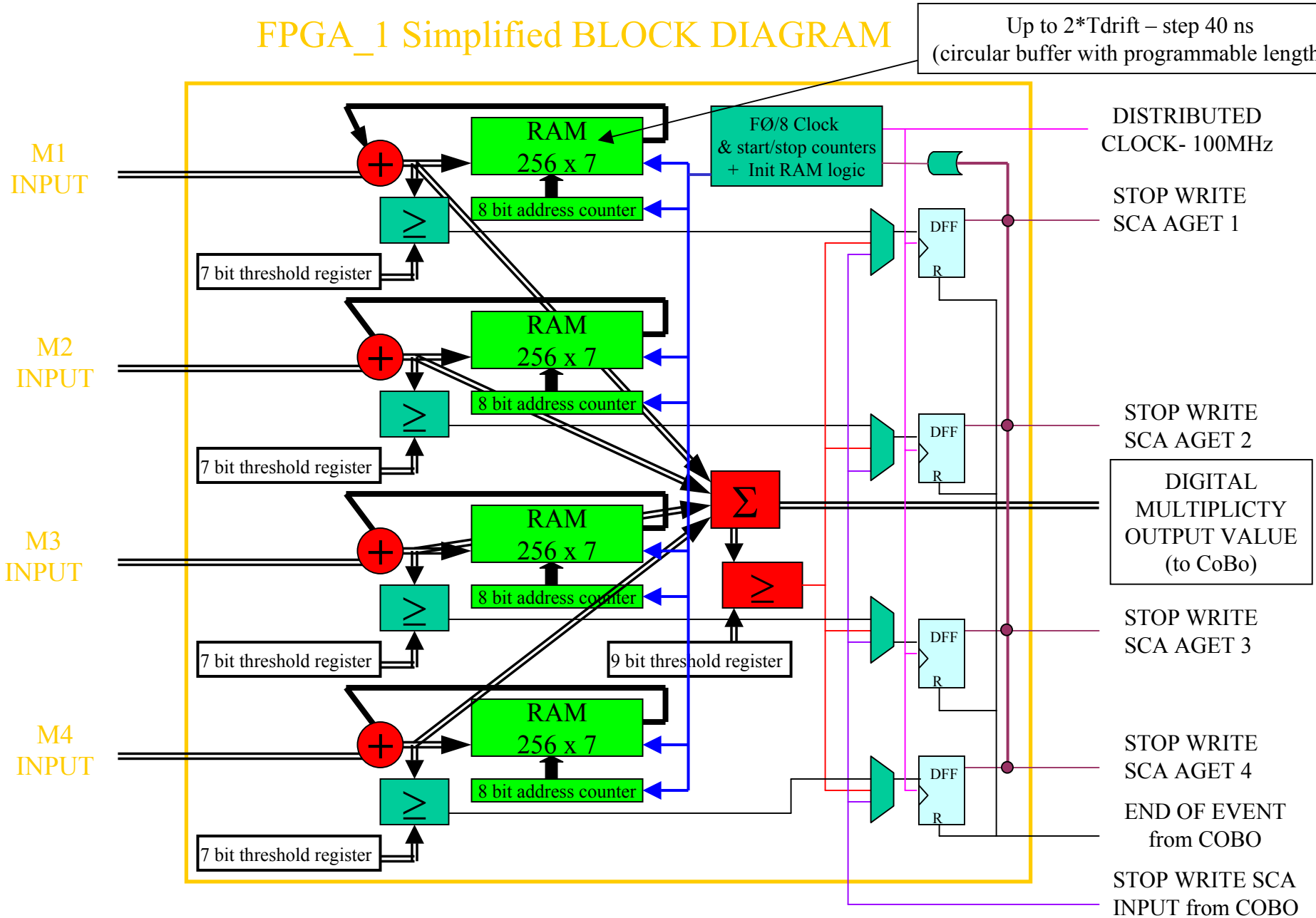
Details of ASAD FPGA

FPGA_1 Simplified BLOCK DIAGRAM



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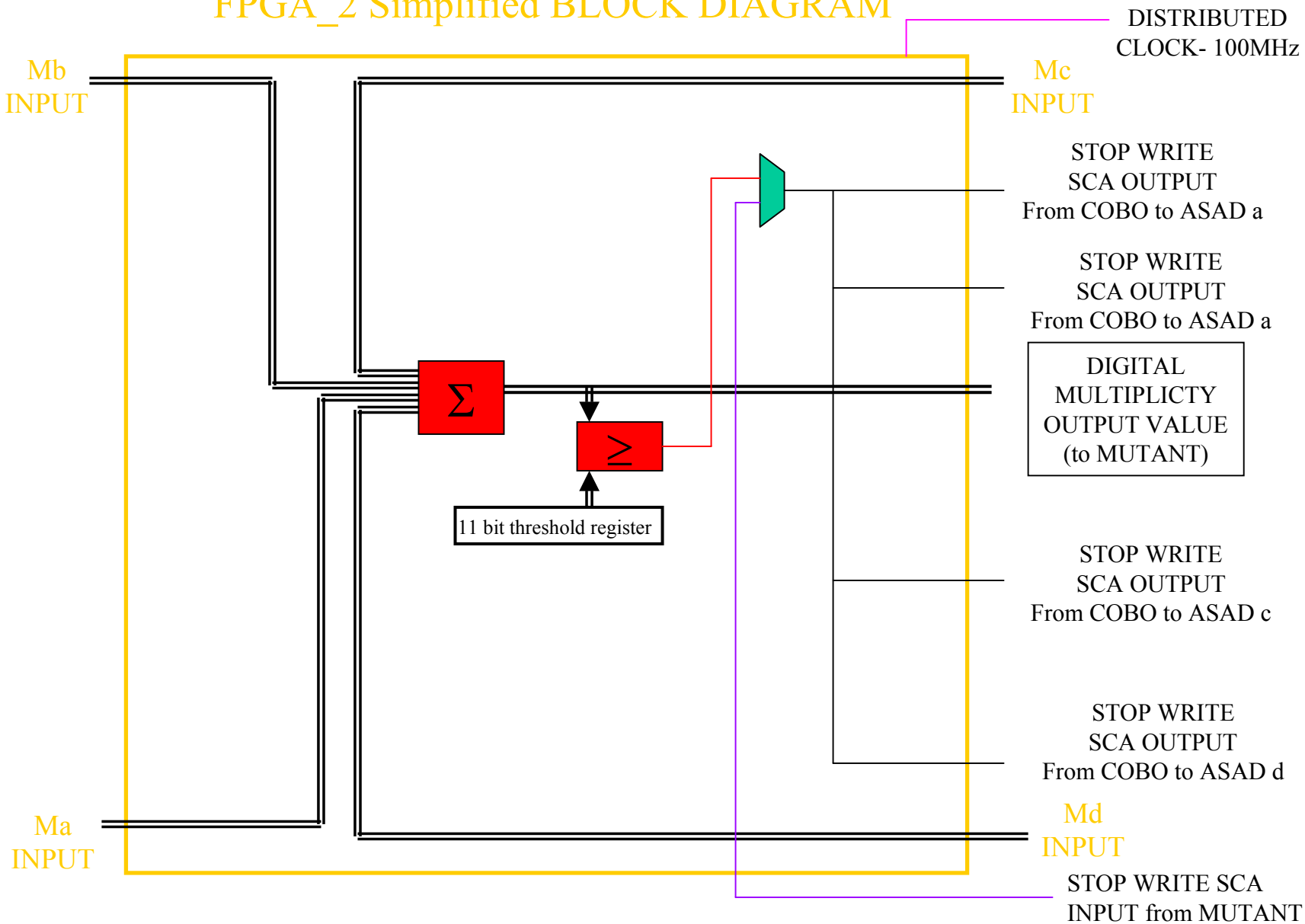
Details of COBO FPGA

FPGA_2 Simplified BLOCK DIAGRAM



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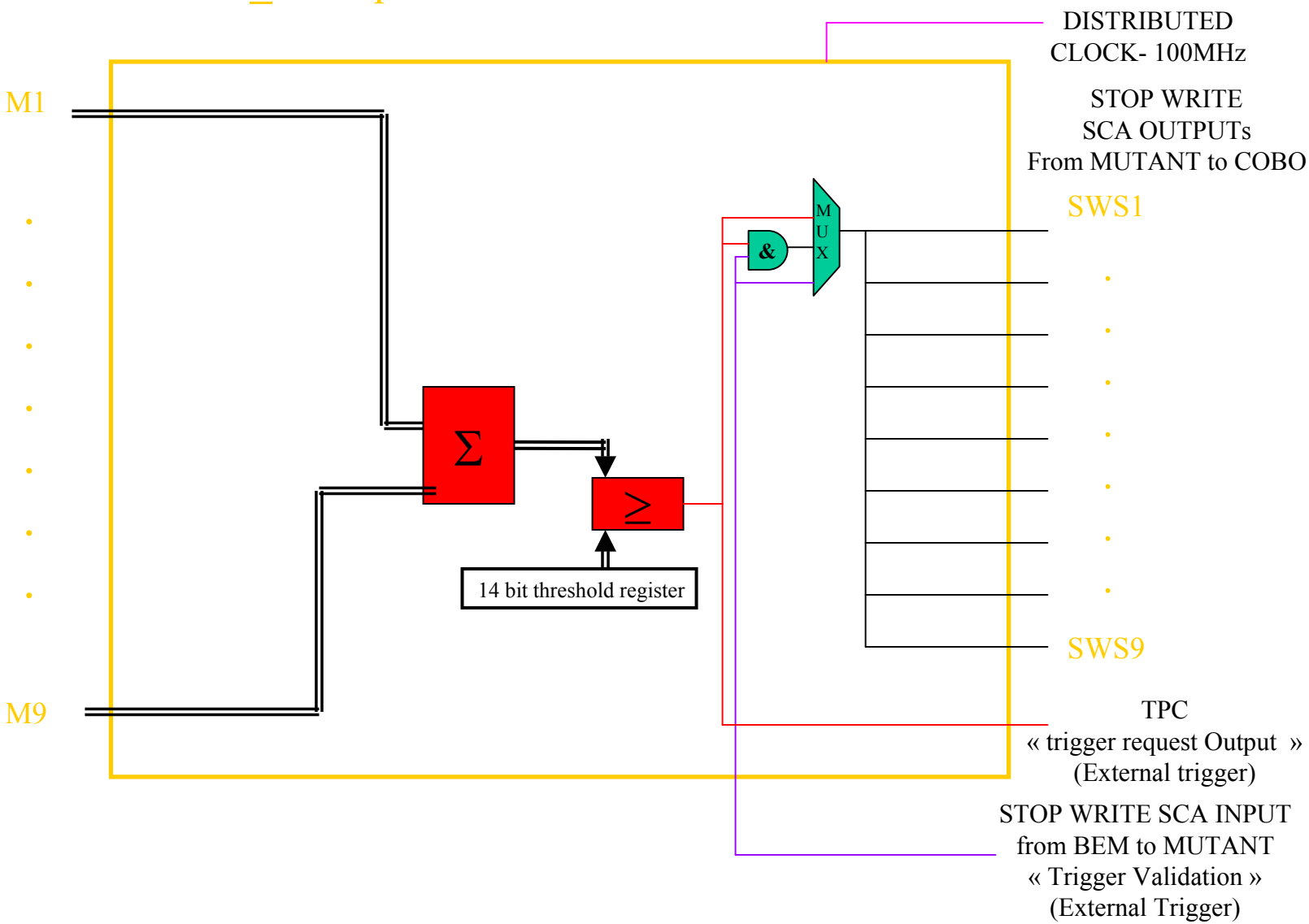
Details of MUTANT FPGA

FPGA_3 Simplified BLOCK DIAGRAM



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