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Commissariat à l'énergie atomique – CEA
Direction des sciences de la matière – DSM

Institut de Recherche Fondamentales sur les lois de l'Univers – IRFU
Service d'électronique, des détecteurs et de l'informatique – SEDI

FRONT END CARD

DESIGN

Abstract.

This document describes the design of the FEC board : its context, the specification it should fulfil, the followed development procedure, its electronic architecture, and its material description : printed circuit, routing layout, mechanical layout and cooling/shielding plates.

Xavier de la Broïse
March 2008

Table of contents.

1 Context.

The architecture for TPC readout consists of two main parts : the on-detector electronics mounted at the back of the gas amplification modules inside the magnet, and the off-detector electronics, housed in standard racks at B2 floor. Each of the two end-plates of the three TPCs comprises 12 Micromegas modules arranged in 2 columns of 6 rows. The on-detector electronics is composed of 72 identical readout modules, it is to say one readout module per Micromegas module. Each of the 72 Micromegas modules is segmented into 48 x 36 pads. It is read out by six Front-End Cards (FEC) and one Front-End Mezzanine (FEM) card as shown in figure 1. Each FEC reads out 288 channels, i.e. a detector area of 48 x 6 pads. Each FEC comprises four custom-made front-end ASIC After (Asic For TPC Electronic Readout). Each ASIC reads out 72 channels, i.e. a detector area of 12 x 6 pads. The After chip samples detector pad signals in a 511-bin switch capacitor array (SCA) at a maximum rate of 50 MHz. The shortest sampling window is ~10 µs which is sufficient for the fastest gas being considered. The FEC is mainly an analog electronic card but it also performs digitization. On the other hand, the FEM is a pure digital electronics card that controls six FEC, gathers event data digitized by the FEC, and interfaces to off-detector electronics. Each FEM has a full-duplex gigabit class optical link to communicate with the off-detector Data Concentrator Cards (DCC). The FEM to DCC path is used to transport event data and some control messages while the DCC to FEM path is used to transport the global clock, trigger and other synchronization signals as well as some protocol and configuration messages. Each FEM is also connected to a daisy-chained slow control network used to gather operating parameters and ensure the safe operation of the read-out electronics. Each readout module has a single low voltage power input. A power cable distributes power to the six FEC and to the FEM. Low voltage power supplies for all on-detector front-end electronics are placed in a rack at B2. The interface between the on-detector electronics and the off-detector electronics consists of 72 duplex optical fibers. Each DCC has 12 duplex fibers and services one TPC end-plate. There are six DCC in the complete system. All DCC are linked to a merger computer that performs a final data reduction and formatting, and communicates with the experiment-wide acquisition system via a standard network connection. The six DCC and the merger computer are housed in a standard, off-the shelf, powered crate. A global view of the complete TPC readout system is depicted in Fig. 2.

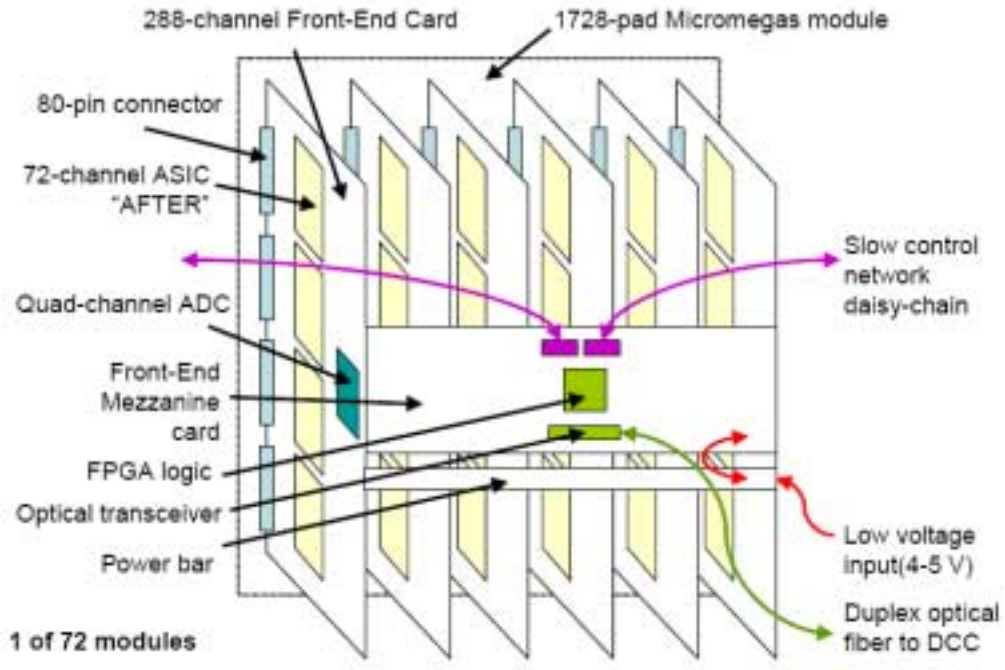


Figure 1 : Read-out module concept.

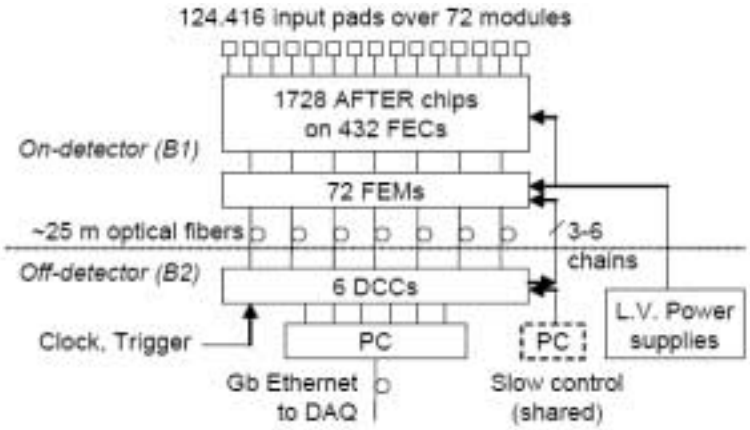


Figure 2 : TPC readout architecture.

2 Specifications.

2.1 Functions.

The Front-End Card (FEC) performs three mains functions (see figure 3) : the numerical conversion of the 288 analogue signals coming from the Micromegas detector, the calibration of this conversion function, and the self-monitoring of the board.

The monitoring consists in measuring some tensions, the supply current and the temperature, and in reading the board identification serial number. In addition, the board links the identification circuit located on the Micromegas detector to the FEM card : it allows this one to read the identification serial number of the detector.

The calibration of the conversion function consists in generating a tension step signal through a capacitance in series to simulate an analogue input signal. The amplitude of this step is well known and is commendable.

The digital conversion of the 288 analogue signals is performed in several stages. The first stage protects the FEC electronics again accidental over voltage coming from the detector. The following stages are the shaping, the analogical storage and the multiplexing (288 → 4) of the signals. They are performed by the After ASIC (see document "ASIC After datasheet", P. Baron and E. Delagnes). At last, the

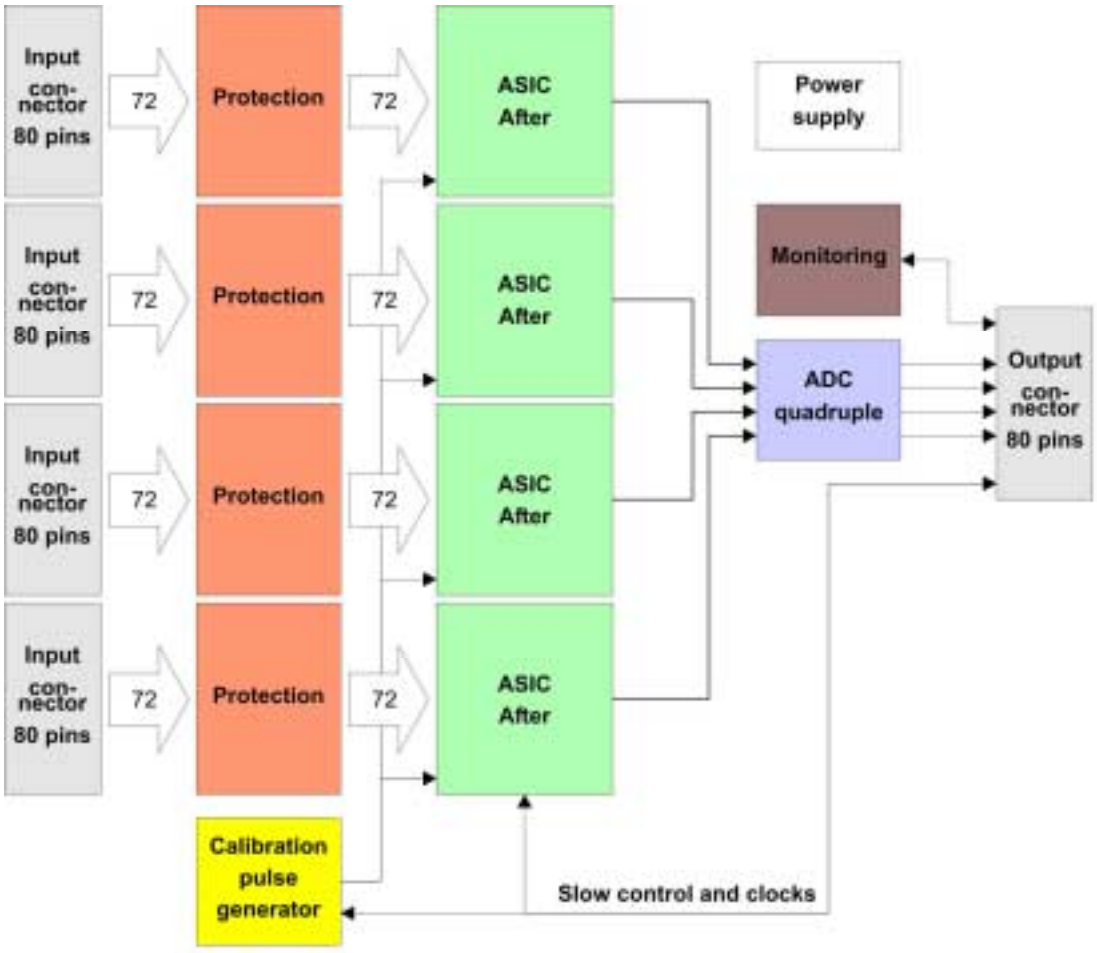


Figure 3 : Schematic diagram of the main functions of the FEC board.

analogue signals is converted into digital values by the quadruple ADC and then sent to the FEM card.

2.2 Requirements.

The global performances required for the 288 analogical channels are the same as those required for the ASIC After. Report to its documentation ("ASIC After datasheet") to have details. The main specification are remained bellow.

Parameter	Value
Number of channels	72
Number of Time bins	511
MIP charge	12fC to 60fC
MIP/noise	100
Dynamic range	10 MIPS on 12bits
Dynamic range (output)	2 V
I.N.L	1% range 0-3 MIPS; 5% range 3-10 MIPS
Gain	Adjustable (4 values)
Sampling frequency	1MHz to 50MHz
Shaping Time	100ns to 2µs
Read out frequency	20 to 25MHz
Polarity of detector signal	Negative (anode of Micromegas TPC end-cap) or Positive (Cathode).
Calibration	Selection 1/72
Test	one internal test capacitor per channel

Figure 4 : List of the After chip requirements.

However, the FEC board should fulfil in addition specific requirements, listed bellow.

The input protection circuits should protect the board components against the short pulses that can be generated by the Micromegas detector when it trips, as well as against long term short circuits between the mesh and a pad of the detector, that put its DC input amplitude to some hundred of volts (until 500 V). Naturally, in this case, the protection should not perturb the detector high voltage supplying and the reading of the other parts of the detector.

Another requirement concerns the routing of the 288 analogue signals from the input connectors: the crosstalk should be of course minimised, but also the capacitance between the trips and the ground plans, to minimise the noise added to the input signals, due to the use of a charge amplifier as input stage.

The precision of the calibration signal is also an important requirement. As already said, a square signal charging a capacitance is used. Its rising time is not critical, because it has no sensible influence on the charge measurement. It only should be clearly lower than the shaping time of the shaping stage (it to say, at less, 100 ns). At the opposite, the precision of the measurement is directly correlated to the precision of the calibration signal amplitude. This one should be better than ±2 %.

Finally, the last requirement concerns the design of the printed circuit and the implementation of components. They should avoid noise perturbations between the analogue and the digital parts of the board.

2.3 Environmental conditions.

The FEC boards will be connected directly on the back of the Micromegas detectors. So they will be located between the TPC itself and the second well, in a stuffy atmosphere (CO_2 in light overpressure) at 22 °C ± 5 °C. The boards should not excessively warm up, nor warm their environment or the gas in the TPC chamber (convection moves can be prejudicial). So these boards should be cooled (figures 5 and 6).

In this area, the density of analogical and numerical electronics will be great and will generates large electromagnetic perturbations. The other parts of the ND280 near detector, like the magnet which generates a constant magnetic field of 0.2 T, will also probably produce electromagnetic perturbations of variable frequencies. So the boards should be equipped with shielding plates.

At last, these boards will be located in areas rarely and not easily accessible, so that the maintenance during the ten years of the experience life will be difficult. So the quality of fabrication of these boards should be strictly controlled.

On the other hand, the boards will not suffer for vibrations nor radiations.

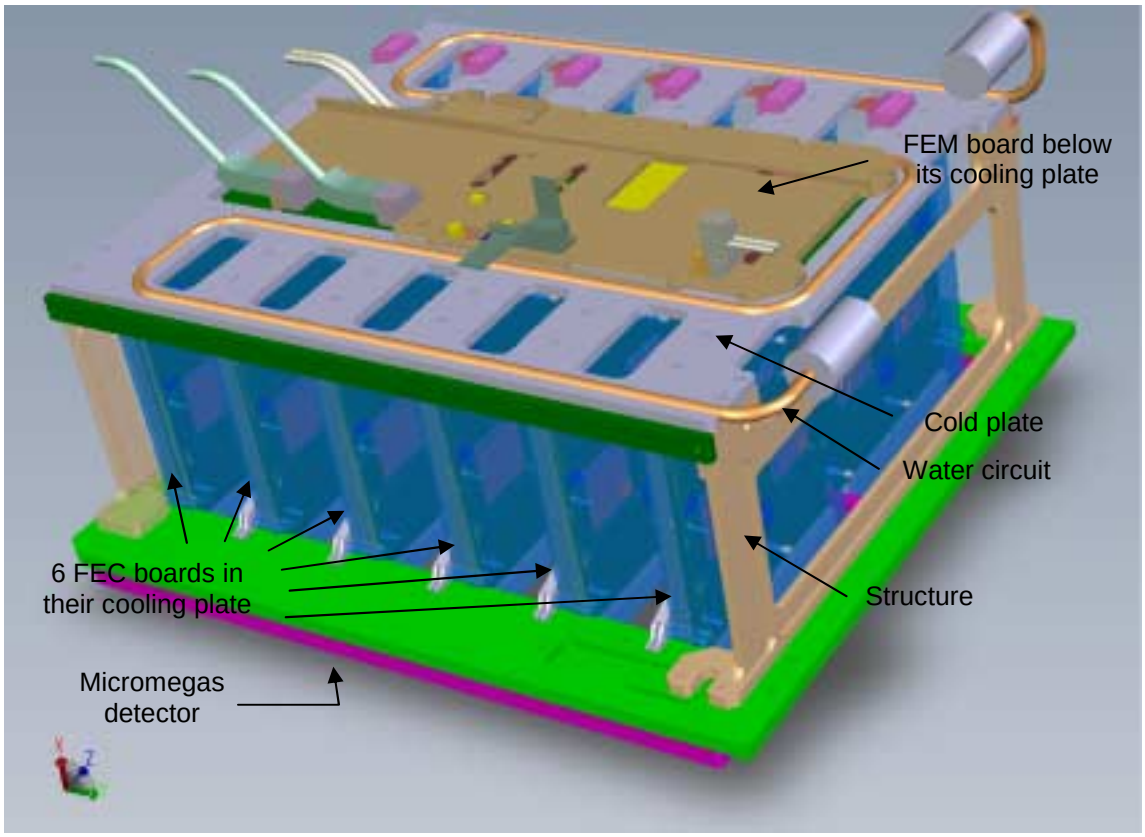


Figure 5 : A detection module : one Micromegas detector, six FEC boards, one FEM board, their shielding and cooling plates, a mechanical structure.

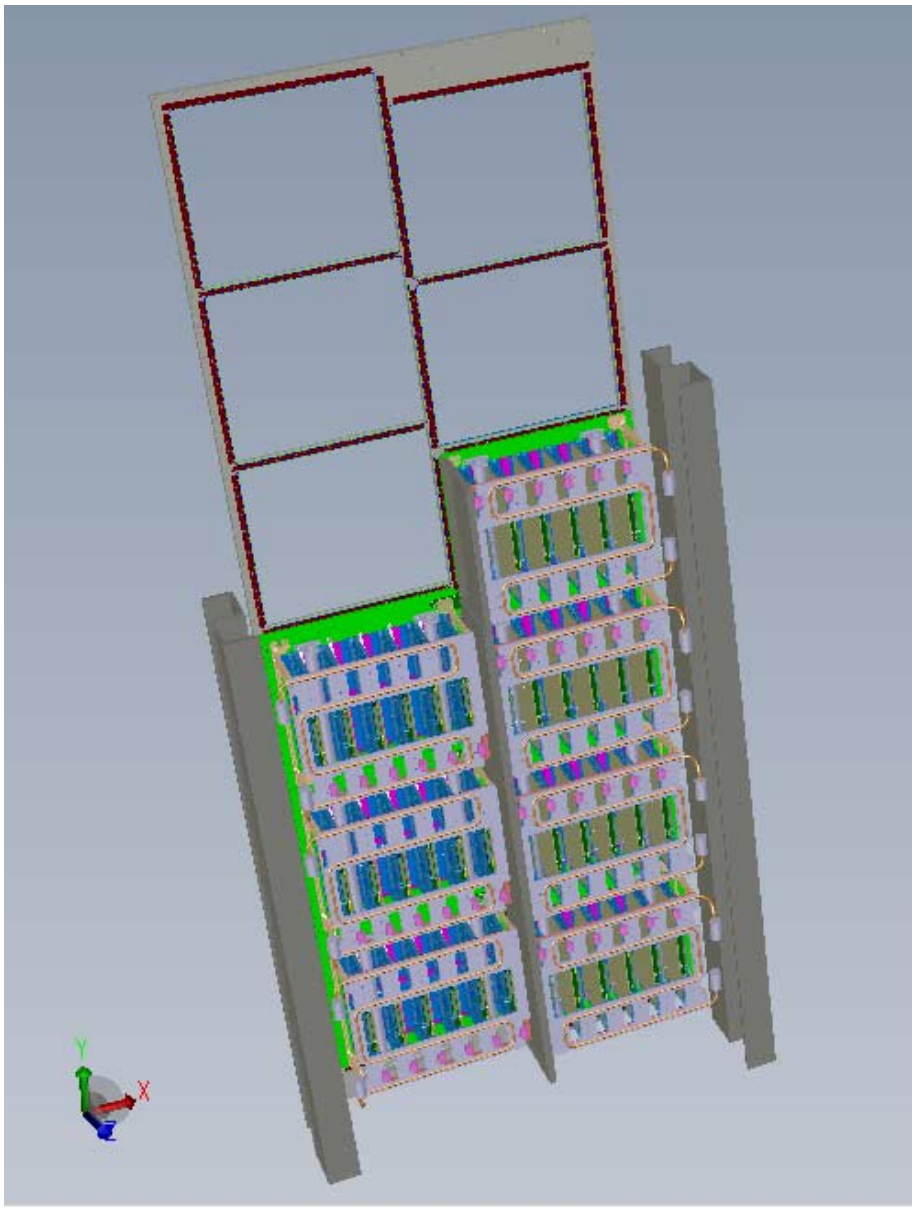


Figure 6 : The detection plan of an half TPC, with the location for 12 detection modules (on this figure only 7 modules are partially equipped with electronics and structure)

3 Development procedure

3.1 Prototyping.

The After ASIC test board (figure 5), which has been developed to test the After ASIC prototype, has been designed to serve too as a pre-prototype of the FEC board. So it included not only the components necessary to validate the ASIC, but also the other functions of the FEC board, as the pulse generator, the self monitoring circuits, two kinds of protection of the inputs, several regulators to compare them, etc. Naturally, the board was designed to not perturb the ASIC validation and characterisation itself with these components that were progressively cabled on the board, or not powered. In addition, the mechanical layout of this board have been made as close as possible (outline, connectors position, etc.) to what was planed at this time for the final FEC board. So this board has been too used to validate some mechanical options of the system (like the quantity of input connectors regarding to the insertion force, the board dimension regarding to the quantity of components to place, etc.). As furthermore it was connectable to the Micromegas detector (the prototypes as the final version), it has been possible to validate the ASIC in true conditions when connected to the detector. It has even been possible to validate and characterise the first prototypes of the Micromegas detectors themselves with an adapted electronics…

The next step of the design has been the fabrication of some tens of true prototypes in order to equip some detection modules during the detector and system tests. Thanks to the work done on the ASIC test board, this first prototype is the final prototype, very close to the production board. So the last step will be directly the serial production board, initialised by a pre-series that will validate the production process.

Figure 7 : The After ASIC test board before the ASICs have been progressively cabled. The socket (at left) allows the successive test of a lot of ASIC.

3.2 Tests.

To validate the design of the board, three kinds of tests have been performed : “on table” functional tests, “on detector” tests, and pre-production validation tests. These tests are described in the document “FEC tests and performances”.

Figure 8 : Photo of the final FEC prototype.

4 Electronic architecture.

This section will describe successively the main functions of the board, to explain how they have been implemented in practice.

4.1 Protection.

▪ ***Schema.***

The protection stage has the double objective to protect the electronics against the sparks in the detectors as well as against a permanent short circuits between the detector mesh and a pad. A first schema (see figure 9) as been studied. It has been tested and validated during the first Harp tests (November 2005). It has the advantage that the diodes are not supplied, and so it avoids any additional noise source on the analogue inputs. But if it fulfils the requirement of protection of electronics against short trips (note that passive components can resist to much higher pulse voltages than DC voltages), it is not convenient against the continuous short circuits.

So another schema should be used (see figure 10). Tests have shown that it does not generate more noise than the previous one (see document "After ASIC tests report"). Using a large resistance (to polarize the detector pad) followed by a capacitance (to isolate it in DC from the electronics), this schema allows the presence of a large DC voltage on the pad without any damage for the electronics. Nevertheless, it imposes that these two components should resist to high DC voltages (until 500 V). This kind of components exists, but are more expensive and larger (resistance CMS 1206 and capacitance CMS 0805). This is in contradiction with the short length of the input trips advised to minimise the noise, but it is necessary. For this same reason of density, to allow the input polarisation of the amplifier, we have chosen to supply one of the diodes rather than to use a second decoupling capacitance. Nevertheless, it imposes a good decoupling of the supply.

▪ ***Choice of the capacitance value.***

The choice of the value C_{dec} of the decoupling capacitance is a compromise between opposite requirements :

- A large value of C_{dec} is needed to favour the charge transfer from the detector to the After ASIC. Indeed it acts as a divider, so that the charge seen by the electronics is only Q_{det} x C_{dec} / (C_{det} + C_{dec}), where Q_{det} is the charge on the detector pad and C_{det} is the capacitance of the detector. Moreover, if C_{det} varies from a channel to another, and it is true in our case because of the difference of length of the signal trips on

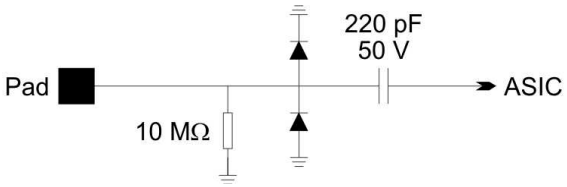


Figure 9 : : First schema of the protection stage (see text)

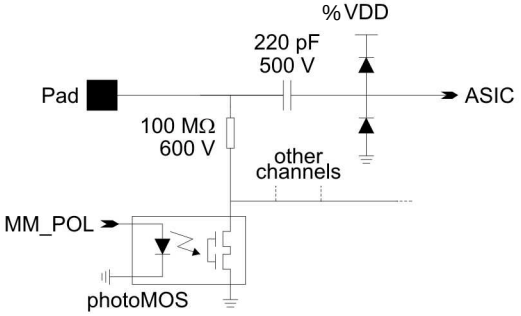


Figure 10 : : Second schema of the protection stage (see text)

the Micromegas PCB, then it induces a variation of the gain of the chain. With C_{dec} = 220 pF, this variation is about 5 %. But as the routing of the detector is known and invariant, this variation can be compensated by calculation.

- A large value improves the crosstalk, as this one is to the first order proportional to C_c / C_{dec}, where C_c is the capacitance inter-pad or inter-strip. With C_{dec} = 220 pF, the crosstalk measured is 1.2 % (see document "FEC tests and performance, section 4.1.3).
- A small value of C_{dec} tends to reduce the died time due to sparks.

The value of C_{dec} = 220 pF has been find to be a good compromise between these requirements.

▪ ***Long term short circuit.***

When a long term short circuit between a detector pad and the mesh occurs, the current through the input resistance can go until 5 µA. This can be a problem for the detector high voltage power supply, especially if several pads are in this case. To avoid perturbing the full detector operation when this occurs, we allow the possibility to remove the connection between the input resistance and the ground plan, and so to make null this current. To this aim, two photoMOS are intercalated each between one-half of the resistances and the mass plan. Each photoMOS is driven by one signal coming from the FEM card. When a photoMOS is put off, one-half (144) of the analogue inputs becomes unreadable.

The photoMOS used (PLA143) has been chosen to have a small off-state leakage current (1 µA maximum at 600 V). Its peak blocking voltage is 600 V maximum.

4.2 Shaping – storage – multiplexing.

These three tasks are performed by four After ASIC, which have been developed for the T2K experiment. Each After ASIC covers 72 FEC analogue inputs, it is to say one fourth of the total number of FEC input (288). So each After ASIC includes 72 channels (figure 11) handling each one detector pad. A channel integrates mainly a charge sensitive preamplifier, an analogue filter (shaper) – see figure 12 – and a 511-sample analog memory. This memory is based on a switched capacitor array structure (SCA), used as a circular buffer in which the analog signal coming out from the shaper is continuously sampled and stored. The sampling is stopped when the external trigger signal come from the FEM board. Then, the 511 samples of each channel are read back, starting by the oldest sample. The analogue data from all the channels are time domain multiplexed toward a single output to be sent to the external 12-bit ADC.

The chip main parameters (gain, peaking time, test mode and ASIC control) are settable by slow control. Two chip inputs permit to calibrate or to test the 72 channels. A "spy" mode is available to control some internal test points (CSA & PZC outputs and SCA input) of the first analogue channel. See the document "ASIC After data sheet" for complete information.

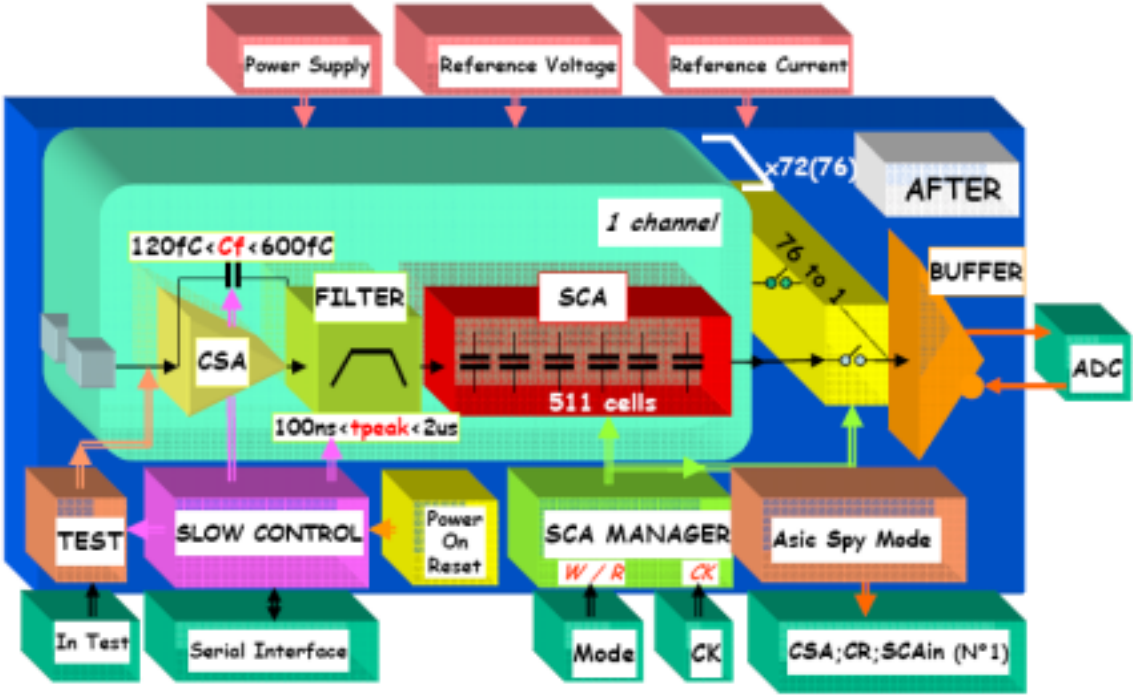


Figure 11 : Block diagram of the AFTER chip.

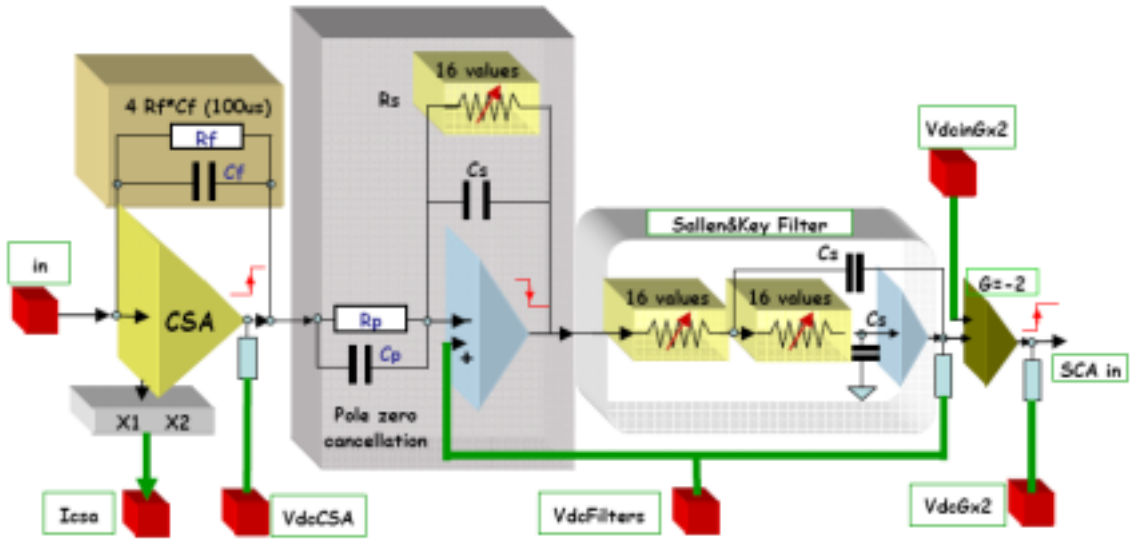


Figure 12 : Schema of the front-end part of an analogue channel : charge sensitive amplifier (C.S.A.), pole-zero cancellation, shaper (Sallen and Key filter) and reversing x 2 gain.

The storage procedure is driven by the Write Clock and the reading procedure by the Read Clock. These two clocks come from the FEM Card. During the reading procedure, the analogue samples of each input channel are successively sent to the next stage to be converted.

4.3 Conversion.

The maximum retention time of the analog signals in the SCA is ~2.5 ms. All front end ASIC must be completely read-out before this volatile information is degraded. Assuming a maximum drift time of ~500 µs for the slowest gas being considered, the time budget that is left for digitization is ~2 ms. To read-out one time bucket in all channels of an ASIC, 79 analogue values are converted. Hence to read-out a complete ASIC, 512 x 79 = 40448 conversions are made in ~2 ms. The minimum conversion rate for

the ADC is therefore ~20 MHz. The required precision is 10-bits. Using commonly found parallel output ADC would lead to a large number of I/O pins (~180-260) for the interface with the FPGA of the mezzanine card. This would need specific attention given the anticipated length of the connection (up to ~15 cm) and could generate excessive switching noise close to sensitive analogue circuits. To solve some of the potential issues of traditional ADC, devices integrating multiple ADCs on a single chip with high speed serial LVDS outputs have been selected. Two candidate devices have been investigated : Analog Devices AD 9229 and Texas Instruments ADS 5240. Both devices are 12-bits resolution quad-channel ADC and operate from a single 3.3 V power supply. Evaluation kits for both devices have been purchased and tested. The Texas part offers more flexibility in test patterns and serialization format. The Analog Devices part has however the decisive advantage of fast re-locking when the sampling clock is suppressed then re-applied. Measurements show that after applying the clock, the AD 9229 and de-serializer logic becomes operational after no more than ~40 µs (over 32.000 trials) while we could not have the ADS 5240 re-lock reliably even after several tens of milliseconds. The AD 9229 has also a wider range of sampling rate (from 10 MHz to 50/65 MHz) while the ADS 5240 cannot operate below 20 MHz. Given the previous considerations, the selected part is AD9229BCPZ-50. This part is lead-free.

4.4 Clock distribution.

To assure a good synchronization between the four ASIC while they perform their sampling task, we use quadruple LVDS repeaters (65LVDS104) for the read and write clock signals (SCA_RCK_P,N and SCA_WCK_P,N. It has the advantage to have a low channel-to-channel output skew : 100 ps maximum, 20 ps typical (the part-to-part skew is 1.5 ns maximum, and the propagation delay between 2.2 and 4.2 ns).

Moreover, the four 100 Ω differential lines linking these repeaters to the four ASIC have been designed to have the same length, to avoid to introduce differences of propagation delay between them.

4.5 Calibration.

The After ASIC includes a test system useful for the electrical calibration of the board, as well as the functionality control of each channels. Three different modes are available : the calibration mode, the test mode and the functionality mode. The calibration operation consists in generating a well known charge at the input of each channel and each ASIC of a FEC board. The charge pulse is generated by a pulse generator on the FEC. In Calibration mode, the generator applies a voltage step to four precision 4.7 pF capacitors (one by ASIC), connected to the In_cal input of the ASIC (pin 39). In other modes (Test and Functionality modes), the generator applies its voltage step directly to the In_testfonc input of the ASIC (pin 40), and the charge injection is created by internal capacitors (whose precision is lower than external capacitances). In all cases, the signal is directed toward the channel(s) to be tested by switches inside the ASIC configured by its slow control (figure 13).

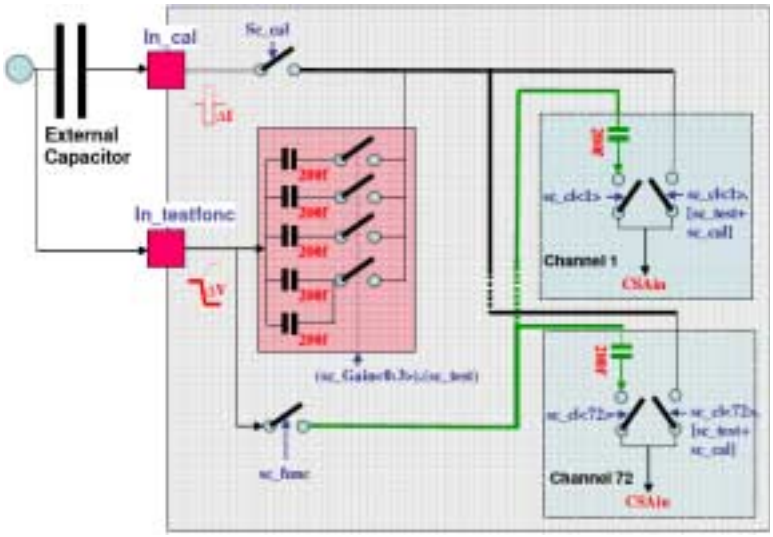


Figure 13 : Schematic of the test system

In the Test mode, four different values of injection capacitor – one by charge range – are used. This allows working with the same test voltage pulse level for the four ranges. The selection of the injection capacitor is automatically done when the charge range is selected. In the Functionality test mode, a single capacitor (200 fF) per channel is used. Whereas for the two first modes only one channel can be selected at a time, for the Functionality mode up to 76 channels can be selected simultaneously. For the FPN channel, only the functionality test is usable.

The rising time of the pulse generator is not critical, because it has no sensible influence on the charge measurement. It only should be clearly lower than the shaping time of the shaping stage (it to say, at least, 100 ns). At the opposite, the precision of the measurement is directly correlated to the precision of the calibration signal amplitude.

The precision of the calibration requires that the rising and falling times are clearly lower than the minimum ASIC shaping time (100 ns), and that the precision is the best possible (better than 2 %). To generate the voltage step, two solutions have been studied. In both cases the square signal of calibration is generated by a digital-to-analogue converter (DAC) followed by a driver. In the first case, the DAC is quick and is able to generate successively and very quickly the high and low levels required to generate a square signal. In the second case, the DAC is slower and so it is used to generate only the high level, a quick switch being used to commute between this high level and the low level which is the ground level.

The following table compares the important features of these solutions. The best options are for the quick DAC the AD9744 by Analog Devices (14 bits), and for the slow DAC the AD5620, AD5640 and AD5660 which are 12, 14 and 16 bits versions of the same family :

Solution with quick DAC (14 bits) :

- Precision :
  - Gain error : ± 0,5 % max
  - Offset error : ± 0,02 % max
  - Integral linearity error : ± 5 LSB max (± 0,8 LSB typ.)
  - External reference : 1,225 V ± 0,16 % max
- Fastness (before ampli) :
  - Propagation delay : 1 ns
  - Settling time (to 0,1 %) : 11 ns
  - Rise time (10 to 90 %) : 2,5 ns
  - Fall time (10 to 90 %) : 2,5 ns
  -
- Price :

Solution with slow lent (12, 14 or 16 bits) :

- Precision :
  - Gain error : ± 0,85 % max
  - Offset error : ± 0,72 % max ; Code zero error : + 0,64 % max
  - Relative precision : ± 4 LSB max (for 14 bits)
  - Internal reference : 1,25 V ± 0,24 % max
- Fastness (before ampli) :
  - Rise time (logic input 50 % to output 90 %) : 7,9 ns
  - Fall time (logic input 50 % to output 90 %) : 4,7 ns

– Register (74HC595) : 2 x 0,3 $
– Voltage reference (AD1580) : 0,68 $ for 1000
– DAC (AD9744) : 7,35 $ for 1000

Total : 8,63 $

• Price :
– DAC (AD5640) : 5,65 $ for 1000
– Quick swich (TS5A2053) : 0,52 $ for 1000

Total : 6,17 $

The second solution have the advantage to offer a serial commend interface, which would allow to connect it directly to the serial control signal coming from the FEM board. At the opposite the first solution implies the implementation of an external register to make the serial/parallel conversion of the control signal. But it is the first solution that has been finally retained (AD9744, 14 bits resolution). The main reason is that its output settling time (to 0.1%) being extremely law (11 ns), it allows avoiding an external commutation chip and thanks to this, the same DAC can be used to fix the two levels of the square signal, and so the offset error becomes strictly null. The maximal integral linearity error is ±5 LSB (±0.8 LSB typ.) and the maximal differential nonlinearity ±3 LSB (±0.8 LSB typ.). So, including the contribution of the voltage reference and of the output driver, the maximal amplitude error can be evaluated to 1.3 %.

This calibration error can be reduced by calibrating the pulse generator itself. To this aim, the output signal is sent to the FEC output connector. The levels will be measured when the FEC boards will be tested before installation, and they will be stored in a database. The only remaining error will then be the maximal differential nonlinearity, it is to say 0,036 % maximum of the full scale value.

To this generator error it should be added the error of the four capacitances (one per After ASIC) where the square signal is injected : ±1 %.

The DAC is driven by a SPI bus that charges the DAC value in two registers (the charged value can be reread as long as no other value has passed through the SPI bus). The SPI protocol is compatible with the slow control protocol of the ASIC, which simplifies and preserves connector pins. The signal “GEN_GO” commands the change of level once the DAC value has been charged. So the time necessary to charge the value limits the frequency of the pulses.

The figure 14 shows the schematic diagram of the pulse generator, conform to the first solution described before. It can be observed that a capacitance *Copt* has been placed at the output of the DAC, to avoid overshoot of the output signal of the generator (GEN_OUT) when the level is changed. The value of this capacitance, 220 pF, has been optimised to avoid lengthening to much the rising and falling times.

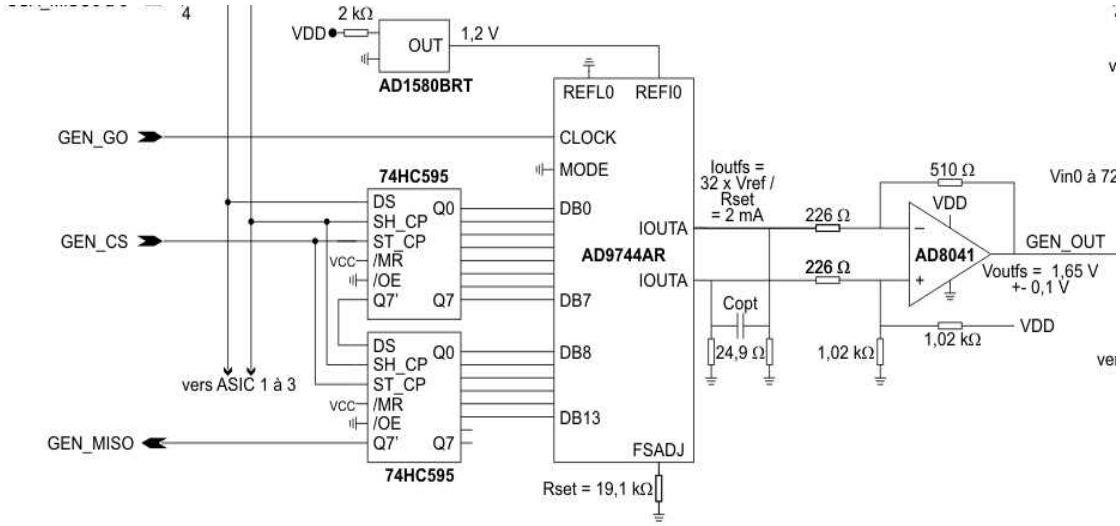


Figure 14 : Schematic diagram of the pulse generator.

4.6 Self-monitoring.

Each FEC card should have a unique identification number for traceability and it is also desirable to monitor local temperature, supply voltage and eventually current. To fulfil these requirements with

minimum hardware, a part in the family of battery management devices from Dallas/Maxim has been selected. These devices provide a 48-bit unique serial number (with an 8-bit family number and an 8-bit CRC), can monitor temperature, voltages, current (depending on version), and use a pin saving 1-wire protocol for communication with the host controller. The DS2438AZ+ brings several other advantages compared to some other parts in the same family. In addition, to measure temperature and power supply voltage, it has a general ADC input which can be useful, and can be powered in parasite mode from the D/Q pin.

So DS2438AZ+ chip has been selected for our board. It contains a temperature sensor and an analogue-to-digital converter that is used to measure the temperature, the power supply, the output pulse generator voltage and the supply current through a 0.1 Ω resistance and an operational amplifier. This operational amplifier is the AD8628AR of Analog Devices. It has been chosen to have the smallest offset voltage (typical 1 µV, maximal 5 µV), so that to induce the smallest possible systematic error on the current measurement. The ratio of the feedback resistances has been chosen so that even if an overvoltage is present on the power supply connector (nominally 4.5 V to 5 V), it does not damage the operational amplifier (powered by 3.3 V).

The DS2438AZ+ can be used even when the card is not powered, but in this case only the serial number functionality becomes available. Then it works thanks to the 1-Wire interface, that can be also used to supply the power to the chip.

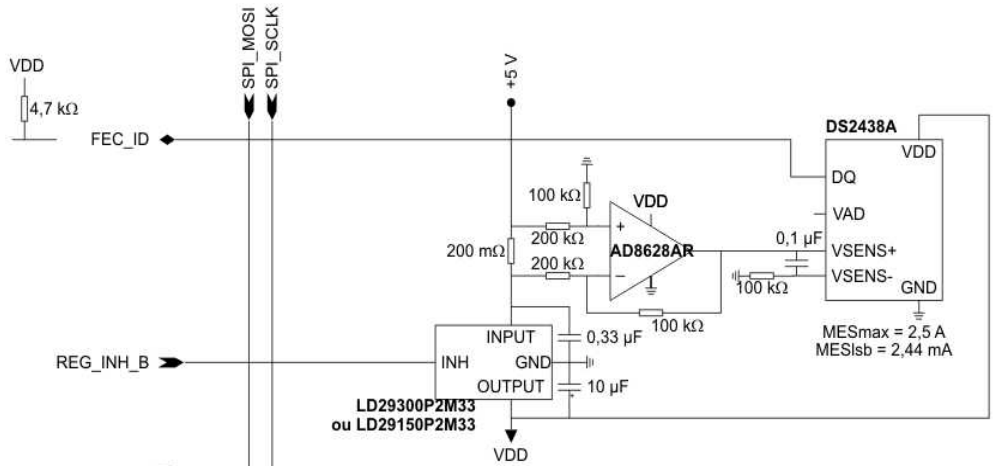


Figure 15 : Schematic diagram of the self-monitoring system.

For tests, an emulator has been developed, in VHDL language, and has been implemented on the FPGA of the reduced FEM (this is a board that emulates one sixth of the FEM board thanks to a FPGA development kit and an adaptation board). In association with the required software in C language that have been also developed, it allows to read the serial number, temperature, voltages and current as it is done by the FEM itself.

4.7 Power supply.

• Regulator.

All the active chips selected for the FEC board can be powered by a **3.3 V** voltage. So one unique regulator can power all the board.

Two regulators have been tested : the LD29150PT33 and the LD29300PT33 by STmicroelectronics. They have been chosen because they put together the features we need : they have both low dropout voltages (0.7 V maximum), fixed output voltage (3.3 V), low noise (132 µV typical), inhibit input, and an internal current limit and thermal limit (150 °C). The only difference between them is the value of the current limit : 1.5 A or 3 A. As the **total current consumption** of the board is finally **between 0.89 A and 0.98 A according to the activity of the board**, we opted for the LD29150PT33 regulator.

• Power supply voltage.

Knowing the dropout voltage of the regulator, a **power supply value of 4.5 V** is widely sufficient. This has the advantage of limit the heat dissipation of the board.

• Protection.

In addition to the protection assured by the regulator itself (current and temperature limitation), and principally to prevent against possible failure of this one, we have placed in series with the power supply connector a Polyswitch resettable "fuse" Tyco ASMD/200-2, whose hold courant[1] is 1.73 A, trip current[2] is 3.93 A, and resistance before trip is 0.07 Ω and after trip and reset is 0.12 Ω maximum. A Vishay S2A diode has been also put to prevent against accidental power inversion (maximum DC blocking voltage : 50 V, maximum average forward rectified current : 1.5 A). At last, this same diode have been put in reverse between the input and the output of the regulator.

• Decoupling.

The regulator datasheet recommends putting at its input a 330 nF capacitance and at its output a 10 µF capacitance. We have followed these recommendation and we have reinforced them adding a set of five 10 µF capacitances in parallel behind the power connector (the place for an 10 µH inductance in series has been also foreseen, but this one will not be cabled because of the inconvenient it would has for other experiences placed in large magnetic field environment, and because it has not prove is utility in T2K context). We have also added two 330 µF capacitances at the output of the regulator (one is placed near the regulator, the other at the opposite of the board).

• Power supply connector.

The power supply connector proposed is the IC 2,5 4-G-5,08 by Phoenix Contact. Its main advantage is that it can support high current (12 A), and so the same connector is able to be used for boards oe cables where large currents pass through, like the power cable. This connector contains four pins, to make possible a redundant cabling. But a two pins version also exists and could be used.

4.8 Inputs – outputs.

4.8.1 Input signals.

The connecting chosen for the 288 analogue inputs is four connectors SMCB 80 F AB VV 6-03 (reference 114806) by Erni. This is 80-pins connectors that have been tested and validated during the first Harp test for T2K (2005). Each connector takes in charge 72 inputs ; four pins at each side are connected to the ground, except one pin of one connector that is connected to the identification chip of the Micromegas detector.

4.8.2 Output signals.

The connector used for the interface between the FEC and the FEM was to be sufficiently robust to survive multiple insertions and removal. Positioning is somewhat critical for the correct insertion of the FEM that has six connectors. The candidate connector was to be available in right-angled version for the final system, but also in straight version for the test bench of the front-end ASIC and the test bench of the FEC. The number of pins was to be sufficient to provide enough grounds for shielding and a few spare pins for signals that were not initially anticipated.

To fulfil these requirements, the connector chosen for the outputs of the FEC card is the FX2-80S-1.27DSL by Hirose. It is a 80-pins connector suitable for high speed signals and more resistant (but less compact) than the input connectors. The corresponding connector on the FEM side is the Hirose FX2CA-80P-1.27DSAL (71), and the RoHS compliant part is referenced 572-2357-7 71.

[1] The largest steady state current that, under specified ambient conditions, can be passed through a PolySwitch device without causing the device to trip.

[2] The smallest steady state current that, if passed through a PolySwitch device, will cause the device to trip, under specified conditions.

4.8.2.1 Principles.

The interface between the FEM card and the FECs is parallel and electrical. Each FEM serves six FEC in the baseline design, but this could be changed to 4 or 8 FEC. The change must be anticipated at design time to minimize the impact on implementation. The interface transports fast LVDS signals (up to 120 MHz DDR), skew, jitter and latency critical signals (ADC and SCA clock and timing signals) and slow control signals. Because the FEM and the FEC will be powered by different voltage regulators, care must be taken to guarantee correct initialization and operation in the following situations. When one or several FEC is powered while the FEM is not yet powered, none of the FEC is allowed to attempt to drive any pin of the interface to a high level. In other words, there must not be any current sourced from the FEC to the FEM through the I/O interface when the FEM is not powered. The same holds true when the FEM is powered but not yet configured (the on-board FPGA I/O's are tri-stated until the firmware has been successfully loaded). Reciprocally, when the FEM is powered while one or several FEC is/are not powered, the FEM is not allowed to source any current to that/these FEC through the I/O interface. This implies that all output signals from the FEM to each FEC is either low or tri-stated in this situation. FEC may be powered off individually, in case of failure for example, or to isolate a mal-functioning FEC. When one or several FEC is/are powered down, the rest of the system must continue to operate normally. This implies that none of the signals distributed from the FEM to the FEC can share a common bus line across all FEC, and all common signals must be buffered on a per FEC slot basis. At the different stages of the development of the system, it will also be useful to run a FEM that is not fully-equipped with all the FEC it would normally serve. This configuration corresponds to the test-bench of the front-end ASIC, the test of one FEC, or the test of partially equipped detector modules. When one or several FEC is not present, the FEM should operate with the actual number of operational FEC, should not distribute any signal to non-present FEC, and must not expect any response from non-present FEC.

4.8.2.2 List of FEM / FEC interface signals

The complete list of interface signals between the FEM and the FECs / front-end ASIC test bench are listed in figure 16 :

Name	Dir.	Standard	Description
General control			
REG_INH_B	I	CMOS 3V3	Power down FEC voltage regulator
ADC_PDWN_B	I	CMOS 3V3	Active low power down for the ADC
MM_POL<1..0>	I	CMOS 3V3	Set half of detector pads to ground or floating (1 for channels 1 to 144, 0 for pads 145 to 288)
SCA control			
SCA_WCK_P	I	LVDS	SCA Write clock ; active on the rising-edge
SCA_WCK_N	I	Tri-state	
SCA_WRITE	I	CMOS 3V3	SCA Write Enable ; active high
SCA_RCK_P	I	LVDS	SCA Read clock ; active on the rising-edge
SCA_RCK_N	I	Tri-state	
SCA_READ	I	CMOS 3V3	SCA Read Enable ; active high
ADC signals			
ADC_CLK	I	CMOS 3V3	ADC clock ; active on rising-edge
ADC_DCO_P	O	LVDS	ADC data clock output
ADC_DCO_N	O	Tri-state	
ADC_DATA_P<3..0>	O	LVDS	ADC serial data output
ADC_DATA_N<3..0>	O	Tri-state	
ADC_FCO_P	O	LVDS	ADC framing clock output
ADC_FCO_N	O	Tri-state	
ADC_DTP	I	Analog	Analog ADC Digital Test Pattern (see Analog Devices AD9229 datasheet for details)
Slow control configuration			
SCA_CS<3..0>	I	CMOS 3V3 Tri-state	Active high Chip Select for each of the 4 ASICs of the FEC
SPI_SCLK	I	CMOS 3V3 Tri-sate	Serial clock input (common to all ASIC and test pulser DAC)
SPI_MOSI	I	CMOS 3V3 Tri-state	Serial data input (common to ASICs and pulser DAC)
SCA_MISO<3..0>	O	CMOS 3V3	ASIC serial data output ; each of the 4 ASIC uses a separate line
Calibration/Test pulser			
GEN_GO	I	CMOS 3V3 Tri-state	Active high Pulser command
GEN_CS	I	CMOS 3V3 Tri-sate	Active high Pulser DAC chip select
GEN_MISO	O	-	Pulser DAC serial data output
GEN_OUT	O	-	Analog output of pulser (for test use)
Monitoring and others			
FEC_ID	I/O	CMOS 3V3 Tri-state	Interface to silicon ID chip, voltage and temperature monitor, using Dallas/Maxim 1-wire protocol
MM_ID	I/O	CMOS 3V3 Tri-state	Silicon ID chip of Micromegas detector
FEC_PR_B	I	CMOS 3V3	FEC presence detection
RES_S<1..0>	I/O	-	For future use

Figure 16 : FEM / FEC interface signal list.

The total number of signals is 41 per FEC, not including grounds and spare signals. The signals listed in figure 16 are required when driving the FEC or the front-end ASIC test bench. Additional signals on the connector being discussed are specific to the test bench of the ASIC and shall not be used on the FEC.

4.8.2.3 Distribution of output signals and multiplexing of input signals

In order to reduce I/O pin count on the FPGA of the FEM, it is not desirable that this FPGA device outputs directly all the signals needed for all FEC. Instead, some repeaters/buffers made with discrete logic are placed at the closest point to the interface connector of each FEC slot. To control easily the distribution of signals on a per FEC slot basis, the FPGA of the FEM produces a FEC_MASK bit pattern (one line per FEC). The FEC_MASK is a pattern read/write-able via slow-control used to enable or disable the distribution/reception of signals to/from each individual FEC. At power-up, and by default after FPGA firmware download, all FEC are masked, and operation cannot start until at least one FEC is un-masked.

See the document “FEM design (Denis Calvet) for conditioning and multiplexing of signals in FEM board.

4.9 Schematic diagram.

A schematic diagram of the board is given (see figure 17). For a complete electronic layout, see section 6.

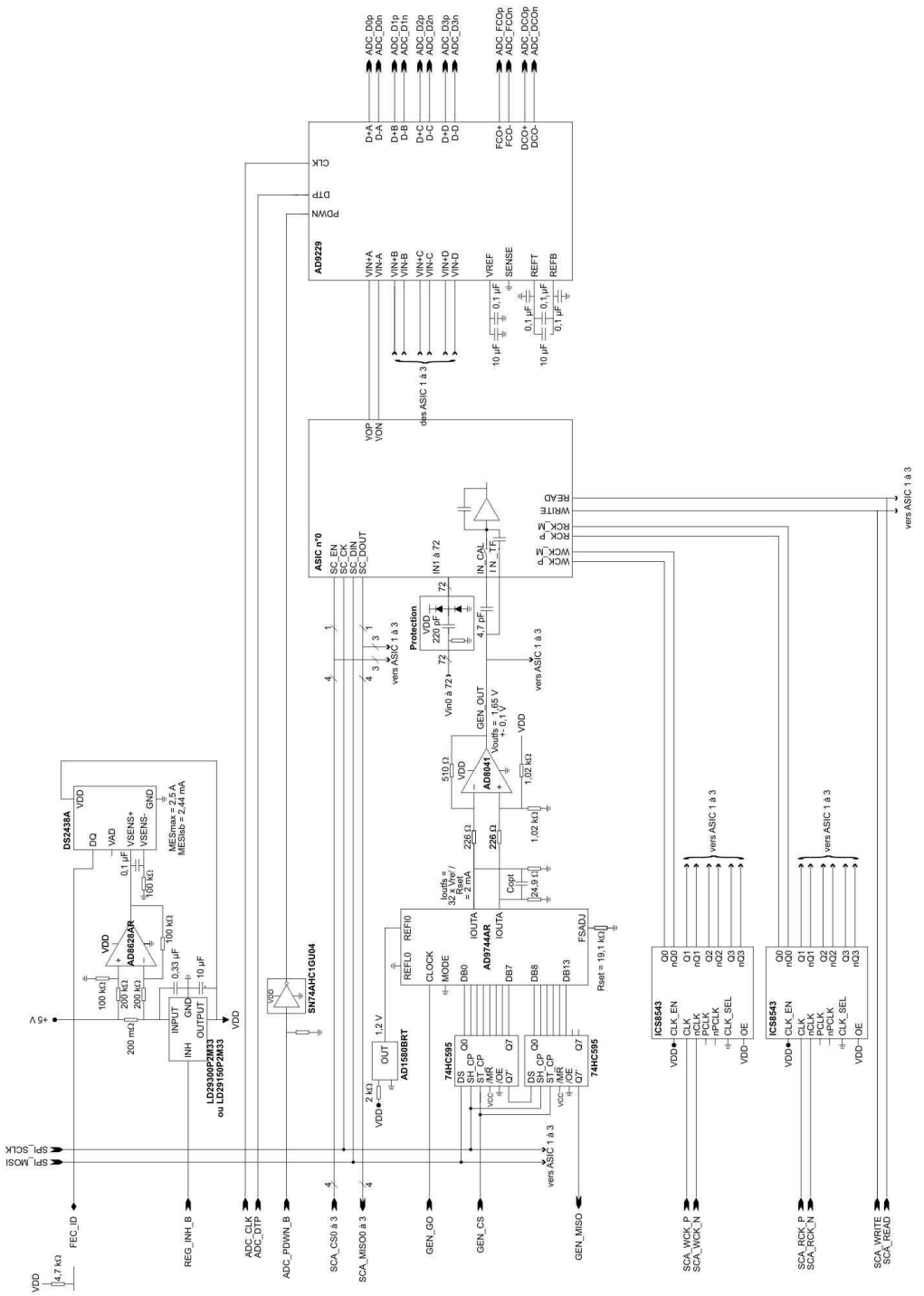


Figure 17 : Complete schematic diagram of the FEC board.

5 Printed circuit.

All the components of the board are ROHS compliant. So the board can be cabled, and will be cabled, following a ROHS process.

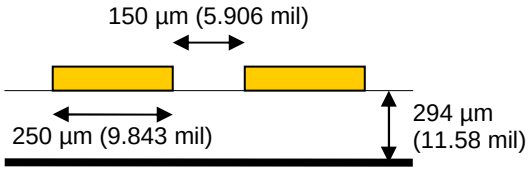
5.1 Dimensions.

The design of the printed circuit of the ASIC prototypes test card has validated the space required for components and routing in the FEC card : 250 mm x 140 mm. Indeed the minimal value for the length of the board (250 mm) is imposed by the length of the four input connectors plus the gap between the two central connectors (this gap is required by a central mechanical piece of the detector structure). The width of the board (140 mm) cannot be noticeably reduced without causing difficulties in PCB routing. The shape of the board outline is shown on the figures of the section 8.1.

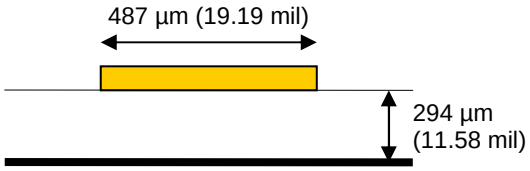
5.2 Lines configuration.

The PCB is planed to be in FR4 HTg. The routing of the lines needs six layers. The package of the integrated circuits used allows us to content with a class V printed circuit. Consequently, the minimal width of lines and the minimal distance between lines is 150 µm. The layer depth should be calculated so that simple 50 Ω and differential 100 Ω microstrips and striplines have the right controlled impedance, while the capacitance between the input lines (in surface) and the ground plans beyond are weak to minimise the noise. The good compromise is about 300 µm depth by layer and a total PCB depth of 1.74 mm. It allows keeping in all configurations reasonable widths of lines, and gaps between lines. The different configuration respected for routing are given bellow, for surface lines and internal lines (for calculation, the value used for ε_r is 4.7) :

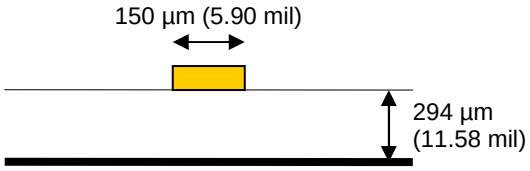
- Surface lines :
  - 100 Ω differential :



  - 50 Ω simple :



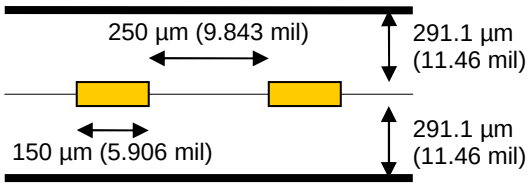
  - Other normal lines :



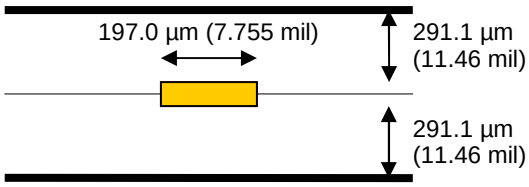
⇒ 85.5 Ω, 1.685 pF/inch

• Internal lines :

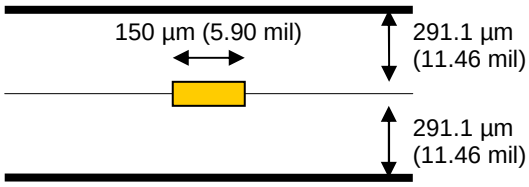
– 100 Ω differential :



– 50 Ω simple :



– Other normal lines :



⇒ 56 Ω, 3.368 pF/inch

The sensible value is the capacitance of the input lines. These ones are routed on surface (top and bottom). In class V printed circuits, the minimal width of these lines is 150 µm. For a 294 µm depth of surface layer, this implies a capacitance of 1.685 pF/inch. As length of the input line is included between 80 mm (= 3.1 inches) and 49 mm (= 1.9 inches), the parasitic capacitance is included between 3.2 pF and 5.2 pF.

If we had selected a surface layer depth of 600 µm (= 23.6 mil) instead of 294 µm, the capacitance would have been reduced to 1.303 pF/inch, and so the input lines capacitances would be included between 2.5 pF and 4.0 pF. But we can see that the gain would be modest (0.7 to 1.2 pF), while the circuit would be thicker and the line dimensions less practical (for example 406 µm between line for differential lines.

So we have kept 294 µm for the depth of surface layers. The capacitance of the input lines have been measured on prototypes, and presented in the document “FEC tests and performances”.

5.3 Stacking up of layers.

In accordance with the layer depth calculating in the previous section, the stacking up bellow have been ask to the manufacturer. It includes 6 layers :

• Top : Input signals + other signals + 50 Ω and 100 Ω differential.
• Gnd1 : Ground layer.
• Alim : Power supply layer + 50 Ω and 100 Ω differential.
• Sig-1 : Signals.
• Gnd2 : Ground layer.
• Bottom : Input signals + other signals + 50 Ω and 100 Ω differential.

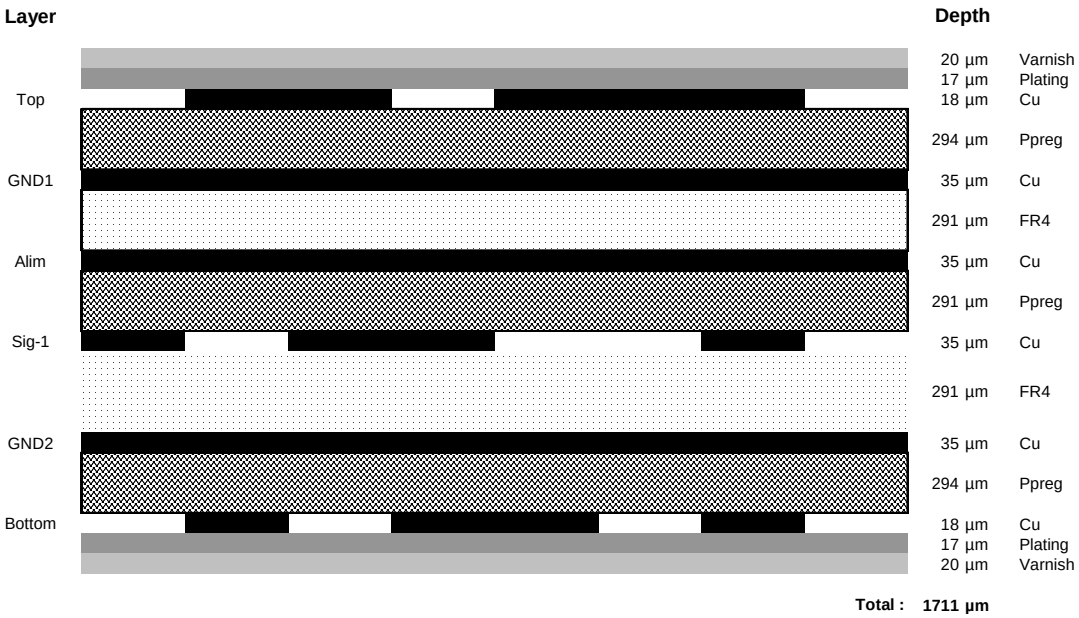


Figure 18 : Optimal stacking-up of PCB layers.

In response to our demand, taking into account the standardised values of layer depth that it had, the manufacturer of our prototypes (Maine CI) have proposed the following stacking up :

COUCHE	TYPE	CUIVRE (*)	SYMBOLES	EPAISSTR	EPAISPPG	STRATIFIE	EPAISDIEL	1080	0106	3313	2116
1	E	45									
					300		300			3	
2	T	35									
				304.8		12 mils	305				
3	T	35									
					300		300			3	
4	T	35									
				304.8		12 mils	305				
5	M	35									
					300		300			3	
6	E	45									
TOTAL		230		609.6	900		1510				

(mm)

Epaisseur totale sur époxy	1.65
Epaisseur totale sur métallisation	1.74

(*) : E = cuivre de base 9 µ + recharge
(*) : L, M ou T = cuivre de base

E = couche externe
L = couche interne logique
M = couche interne masse
T = couche interne tension

====		cuivre "externe"
-------		cuivre "interne"
		préimprégnés
		stratifiés

Figure 19 : Layer stacking-up proposed by the prototype PCB manufacturer.

6 Electronic layout.

6.1 Output connector pin-out.

The following table gives the allocation of pins for the signals between the FEC board and the FEM board. See section 4.8.2.2 to know the function of each signal. The principle of the allocation has been to spread the ground pins, and to do so that the ground pins are preferentially located at the “top” location of the right angle connector, so that they make a kind of shielding upon the active pins.

	Use	Name	Top connector side	PCB side	Name	Use	
		GND	a40	b40	GND		
	µM polaris.	MM_POL0	a39	b39	MM_POL1	µM polaris.	
		GND	a38	b38	GND		
		GND	a37	b37	SCA_WCK_N	SCA	LVDS
		GND	a36	b36	SCA_WCK_P	SCA	LVDS
CMOS	SCA	SCA_READ	a35	b35	SCA_WRITE	SCA	CMOS
		GND	a34	b34	SCA_RCK_N	SCA	LVDS
		GND	a33	b33	SCA_RCK_P	SCA	LVDS
		GND	a32	b32	GND		
	SCA	SCA_MISO0	a31	b31	SCA_MISO1	SCA	
	SCA	SCA_MISO2	a30	b30	SCA_MISO3	SCA	
		GND	a29	b29	GND		
	SCA	SCA_CS0	a28	b28	SCA_CS1	SCA	
	SCA	SCA_CS2	a27	b27	SCA_CS3	SCA	
		GND	a26	b26	GND		
	FEC presence	FEC_PR_B	a25	b25	MM_ID	µM serial nb	
	ADC	ADC_DTP	a24	b24	ADC_PDWN_B	ADC	
		GND	a23	b23	GND		
		GND	a22	b22	ADC_DCO_P	ADC	LVDS
		GND	a21	b21	ADC_DCO_N	ADC	LVDS
		GND	a20	b20	ADC_FCO_P	ADC	LVDS
		GND	a19	b19	ADC_FCO_N	ADC	LVDS
		GND	a18	b18	GND		
		GND	a17	b17	ADC_DATA_P0	ADC	LVDS
		GND	a16	b16	ADC_DATA_N0	ADC	LVDS
		GND	a15	b15	ADC_DATA_P1	ADC	LVDS
		GND	a14	b14	ADC_DATA_N1	ADC	LVDS
		GND	a13	b13	ADC_DATA_P2	ADC	LVDS
		GND	a12	b12	ADC_DATA_N2	ADC	LVDS
		GND	a11	b11	ADC_DATA_P3	ADC	LVDS
		GND	a10	b10	ADC_DATA_N3	ADC	LVDS
	Bus SPI	SPI_SCLK	a9	b9	GND		
	Bus SPI	SPI_MOSI	a8	b8	ADC_CLK	ADC	CMOS
		GND	a7	b7	GND		
	DAC	GEN_OUT*	a6	b6	GEN_CS	DAC	
	DAC	GEN_MISO	a5	b5	GEN_GO	DAC	
		GND	a4	b4	GND		
	FEC serial nb	FEC_ID	a3	b3	REG_INH_B	Regulator	
	Reserve	RES_S0	a2	b2	RES_S1	Reserve	
		GND	a1	b1	GND		

Notes :

***GEN_OUT : Calibration generator output signal. Will be used only by the FEC test bench (and not by the FEM) to measure and store in database the signal levels. The precision of the calibration will be so improved by knowing the card to card variations of generator levels.**

Figure 20 : Output connector pin-out.

6.2 Input connector pin-out.

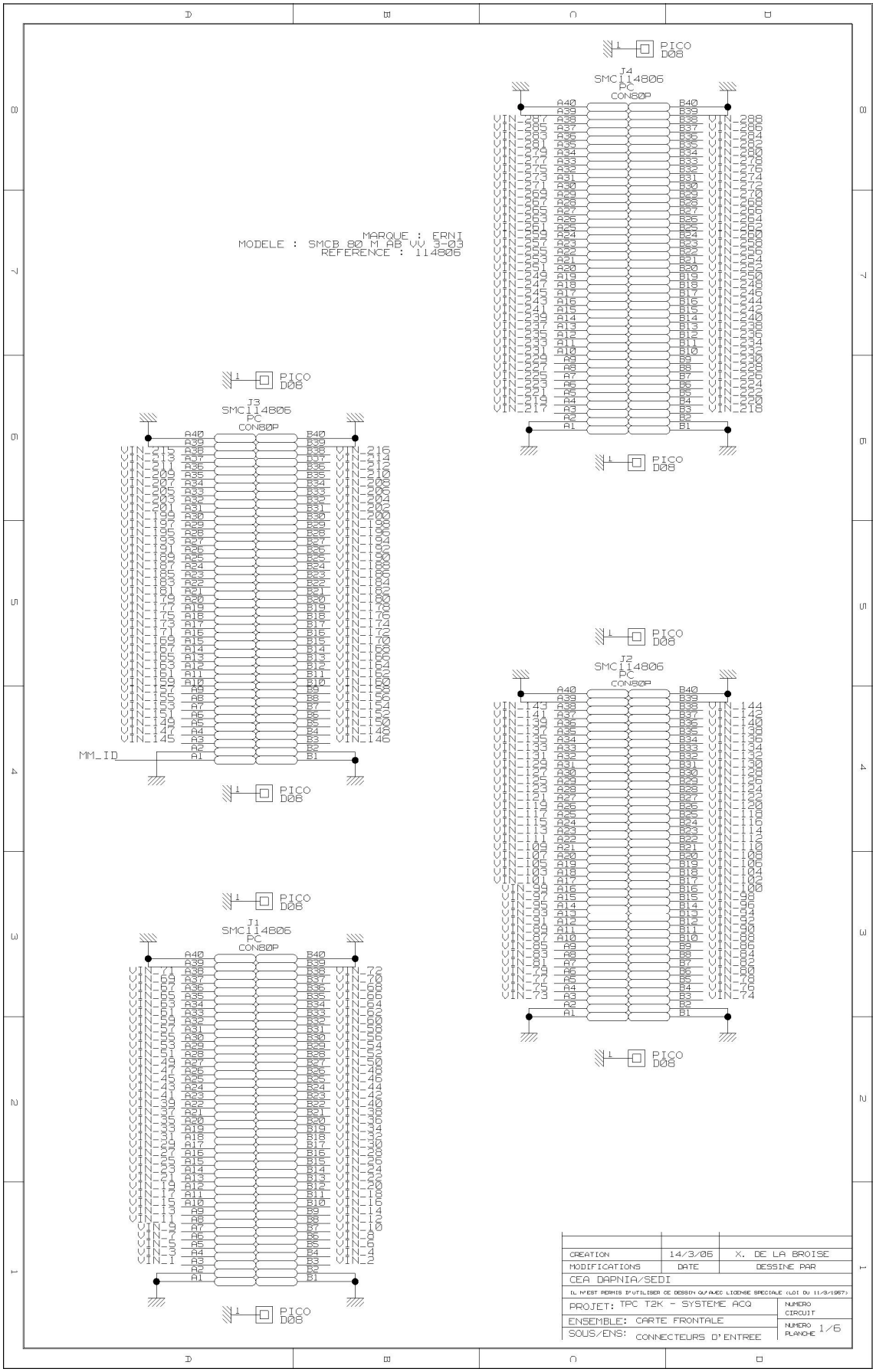
Each of the four input connectors (it is to say the connectors between the detector and the FEC board) have eight pins to the ground : four at each side (pins A1, B1, A2, B2, A39, B39, A40, B40), except the pin A1 of the connector J3 which receives the signal MM_ID that comes from the detector. The other pins are devoted to the analog channels :

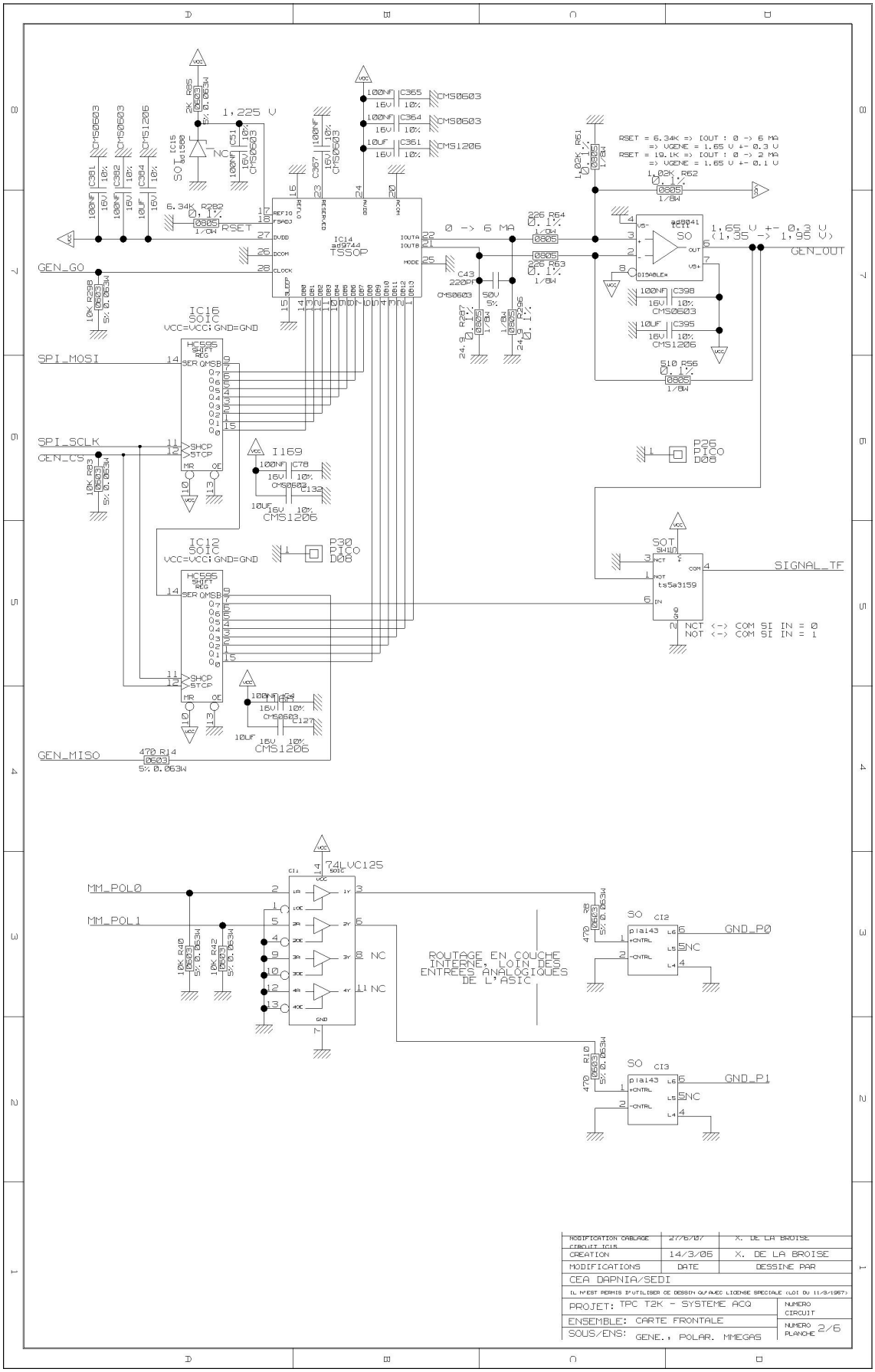
- connector J1 : channels 1 to 72,
- connector J2 : channels 73 to 144,
- connector J3 : channels 145 to 216,
- connector J4 : channels 217 to 244.

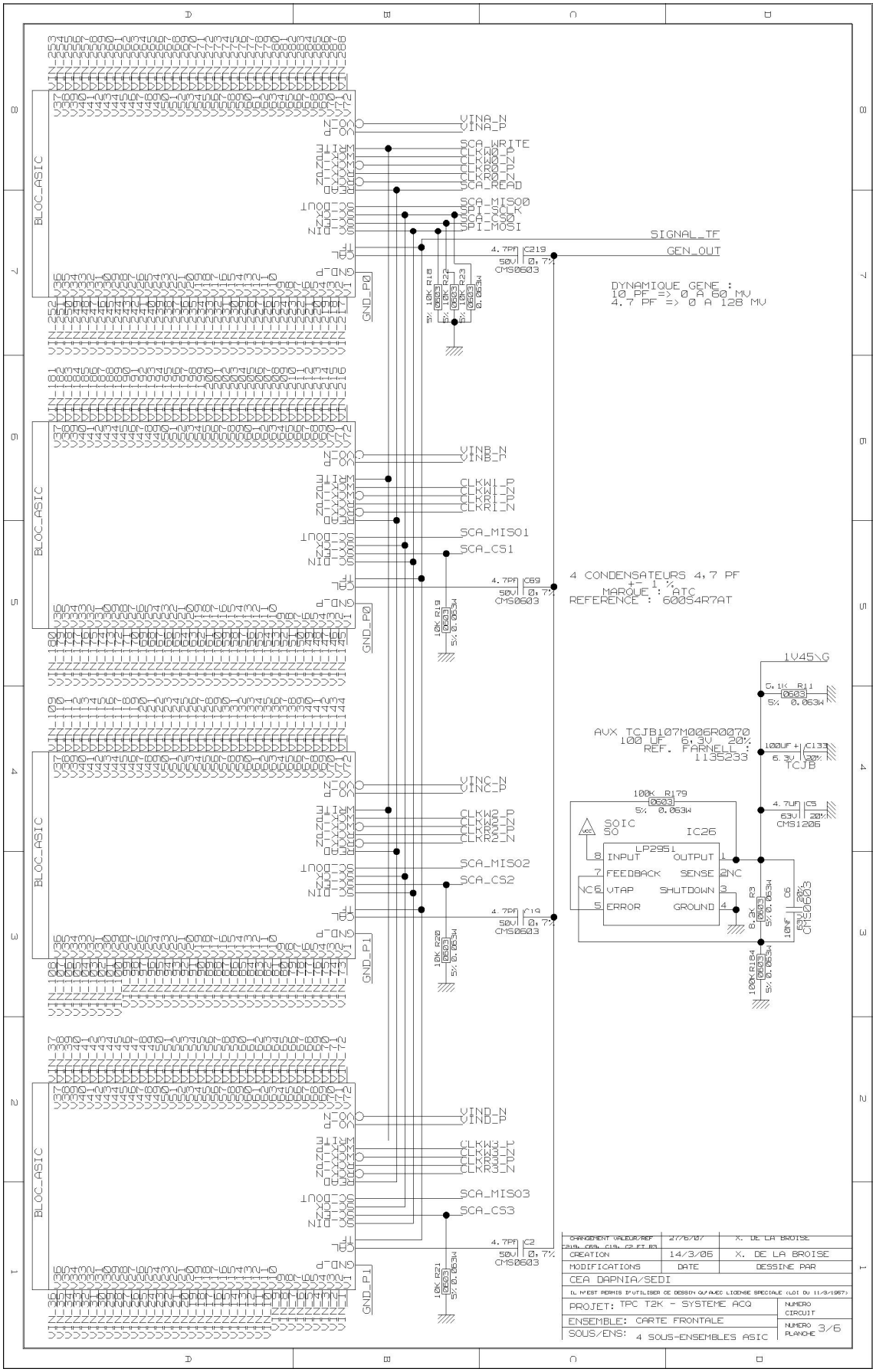
6.3 Electronics.

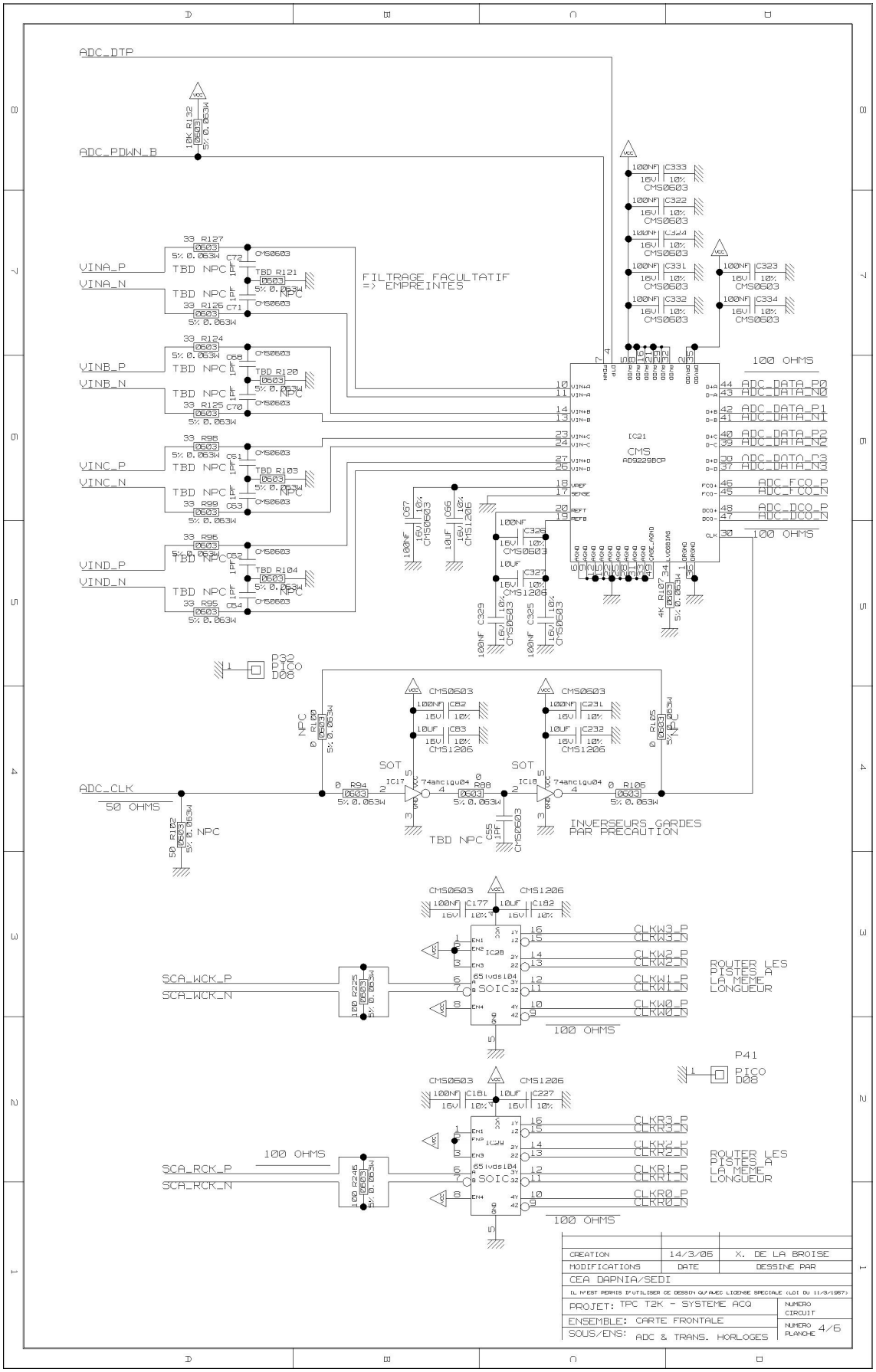
The following pages give the complete electronic layout of the FEC board. All the components commented “NPC” will have their corresponding pads on the printed circuit, but will be not effectively cabled.

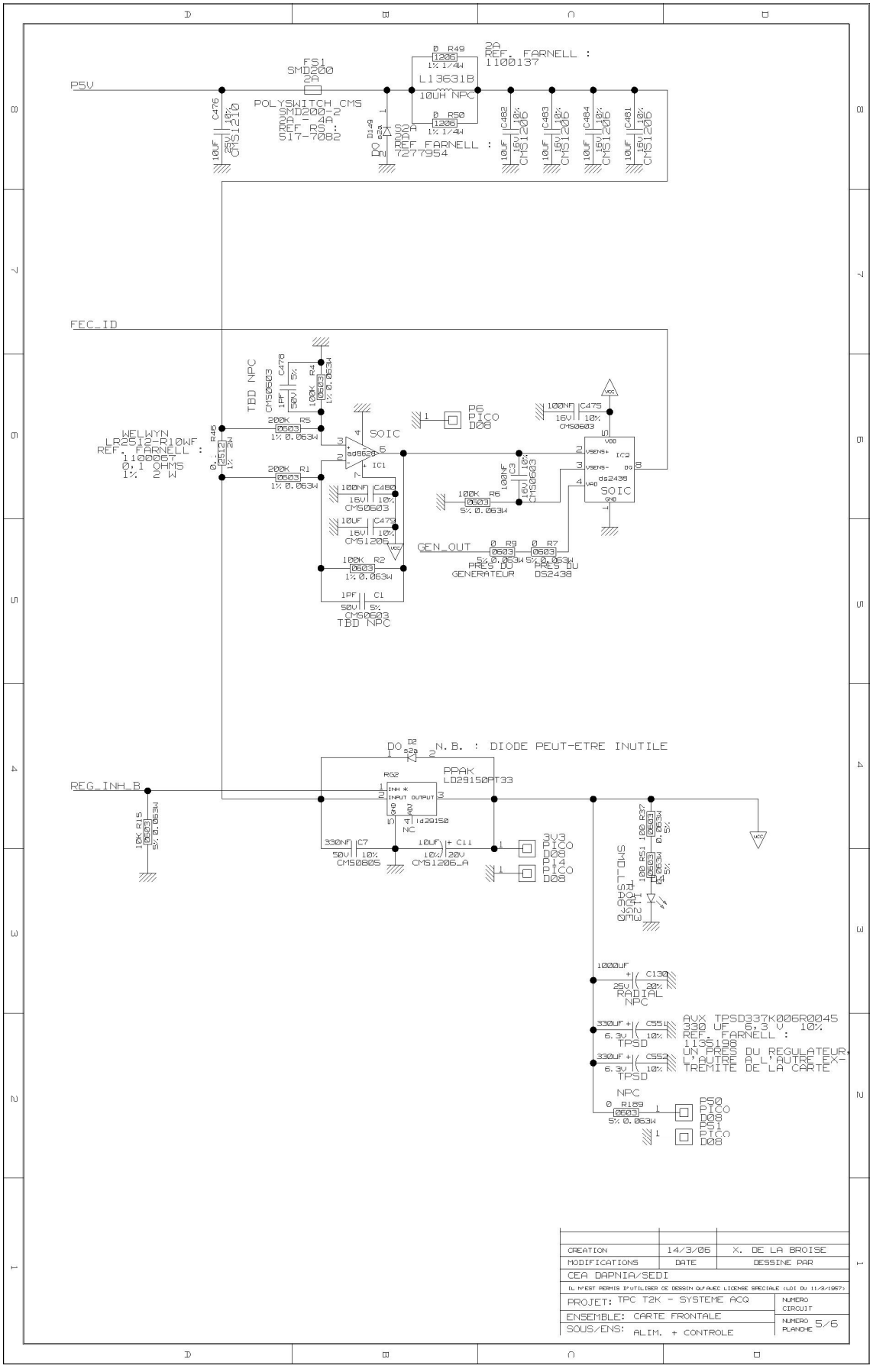
- First page (sheet 1/6) : Input connectors.
- Second page (sheet 2/6) : Pulse generator and command of detector pads polarisation.
- Third page (sheet 3/6) : Cabling of the four analog cells.
- Fourth page (sheet 4/6) : ADC and clock transmission.
- Fifth page (sheet 5/6) : Power supply and self-monitoring.
- Sixth page (sheet 6/6) : Output connector and power supply connector.
- Seventh page (sheet A1/2) : Protection part of the ASIC block.
- Eighth page (sheet A2/2) : ASIC part of the ASIC block.
- Ninth page (sheet B1/1) : Protection block.

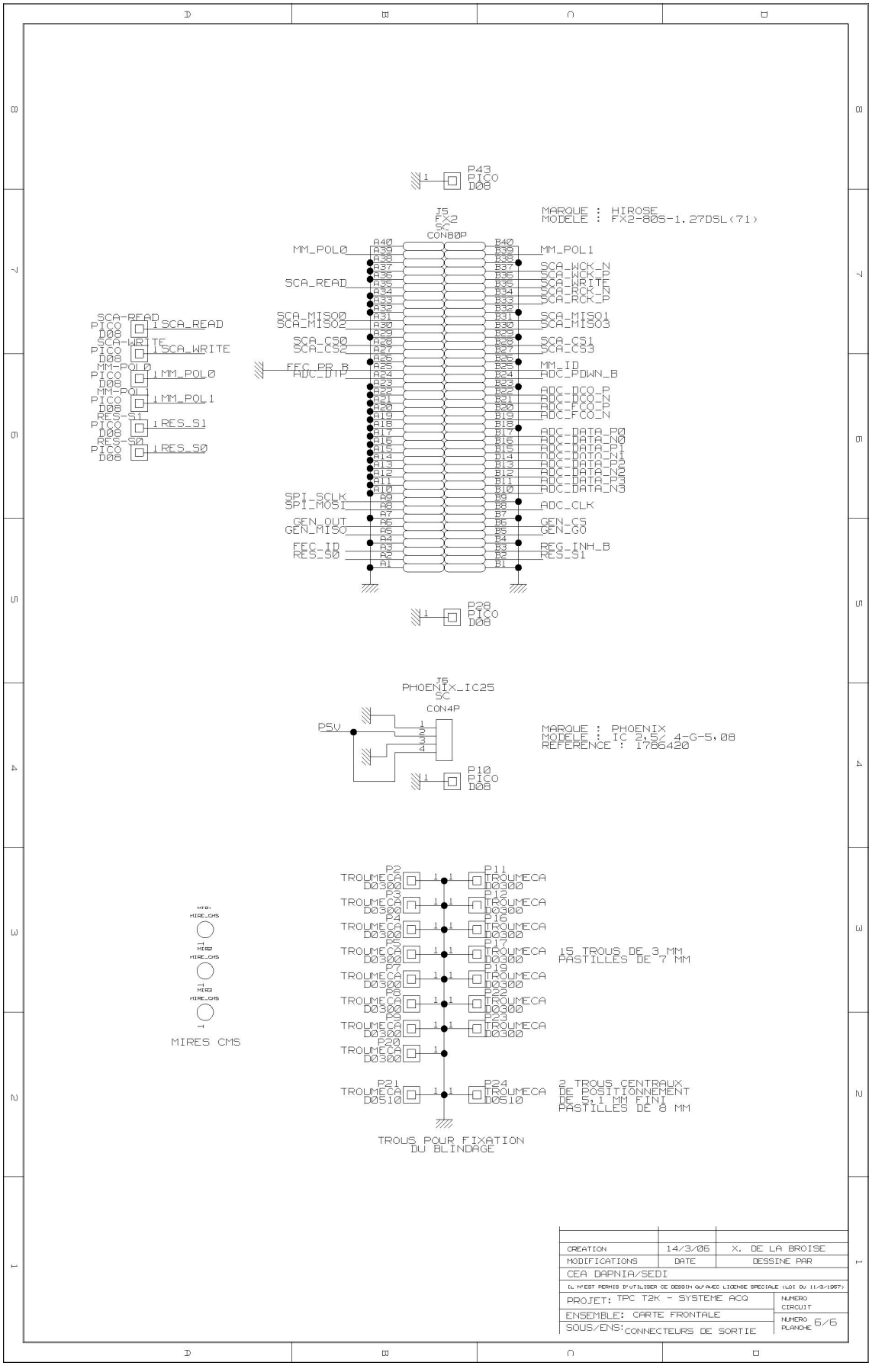

MARQUE : ERNI
MODELE : SMCB 80 M AB VV 3-03
REFERENCE : 114806
J4
SMCI14806
PC
CON80P
J3
SMCI14806
PC
CON80P
J2
SMCI14806
PC
CON80P
J1
SMCI14806
PC
CON80P
PICO
D08
MM_ID
CREATION
14/3/06
X. DE LA BROISE
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
PROJET: TPC T2K - SYSTEME ACQ
ENSEMBLE: CARTE FRONTALE
SOUS/ENS: CONNECTEURS D'ENTREE
NUMERO CIRCUIT
NUMERO PLANCHE 1/6


1,225 V
RSET
GEN_GO
SPI_MOSI
SPI_SCLK
GEN_CS
GEN_MISO
IC16
IC17
VCC=VCC; GND=GND
Ø -> 6 MA
1,65 V +- 0,03 V
(1,35 -> 1,95 V)
GEN_OUT
SIGNAL_TF
NCT <-> COM SI IN = Ø
NOT <-> COM SI IN = 1
P25
P30
MM_POL0
MM_POL1
74LVC125
ROUTAGE EN COUCHE
INTERNE, LOIN DES
ENTREES ANALOGIQUES
DE L'ASIC
GND_P0
GND_P1
CEA DAPNIA/SEDI
PROJET: TPC T2K - SYSTEME ACQ
ENSEMBLE: CARTE FRONTALE
SOUS/ENS: GENE., POLAR. MMEGAS
CREATION 14/3/06 X. DE LA BROISE
MODIFICATIONS DATE DESSINE PAR
NUMERO PLANCHE 2/6

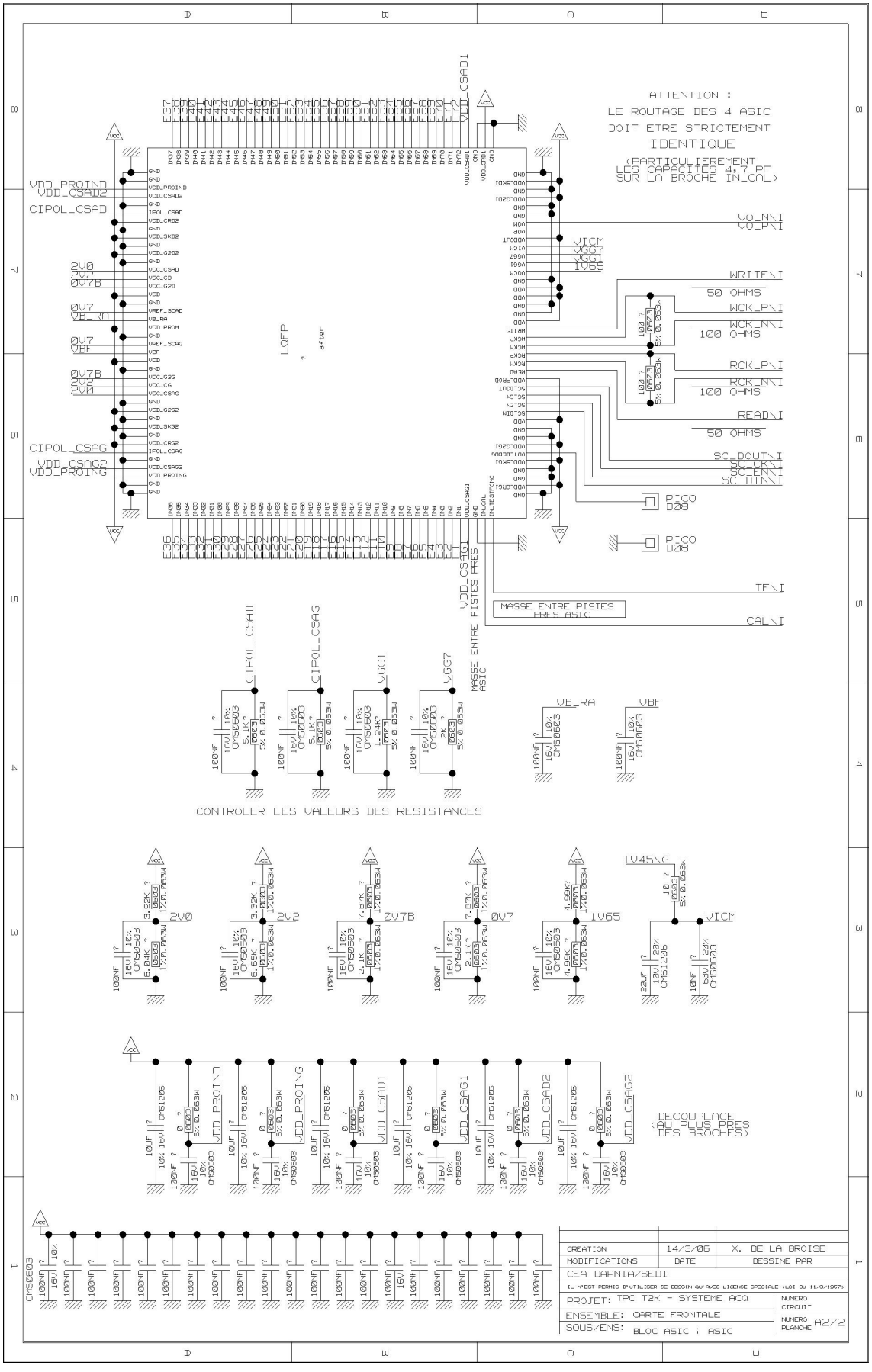

BLOC_ASIC
VINA_N
VINA_P
SCA_WRITE
SCA_READ
SCA_MISO0
SPI_SCLK
SCA_CS0
SPI_MOSI
SIGNAL_TF
GEN_OUT
4.7PF C219
50V 0.7%
CMS0603
GND_P0
5% 10K R18
10K R22
10K R23
0.063W
DYNAMIQUE GENE :
10 PF => 0 A 60 MV
4.7 PF => 0 A 128 MV
VINB_N
VINB_P
SCA_MISO1
SCA_CS1
4.7PF C69
4 CONDENSATEURS 4,7 PF
+- 1%
MARQUE : ATC
REFERENCE : 60054R7AT
10K R19
VINC_N
VINC_P
SCA_MISO2
SCA_CS2
4.7PF C19
10K R20
GND_P1
VIND_N
VIND_P
SCA_MISO3
SCA_CS3
4.7PF C2
10K R21
1V45\G
5.1K R11
AUX TCJB107M006R0070
100 UF 6.3V 20%
REF. FARNELL :
1135233
100UF + C133
TCJB
100K R179
4.7UF C5
63V 20%
CMS1205
SOIC
SO
IC26
LP2951
INPUT
OUTPUT
FEEDBACK
SENSE
VTAP
SHUTDOWN
ERROR
GROUND
8.2K R3
10NF C6
100K R184
CHANGEMENT VALEUR/REF 27/6/07 X. DE LA BROISE
CREATION 14/3/06 X. DE LA BROISE
MODIFICATIONS DATE DESSINE PAR
CEA DAPNIA/SEDI
PROJET: TPC T2K - SYSTEME ACQ
ENSEMBLE: CARTE FRONTALE
SOUS/ENS: 4 SOUS-ENSEMBLES ASIC
NUMERO CIRCUIT
NUMERO PLANCHE 3/6

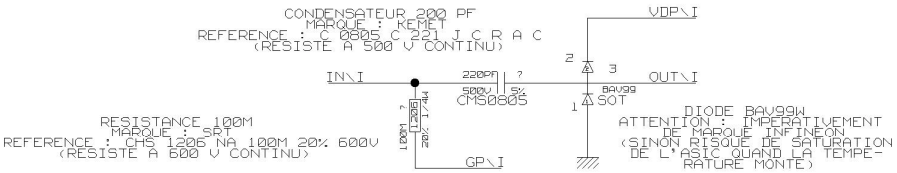

ADC_DTP
ADC_PDWN_B
VINA_P
VINA_N
VINB_P
VINB_N
VINC_P
VINC_N
VIND_P
VIND_N
FILTRAGE FACULTATIF
=> EMPREINTES
100 OHMS
ADC_DATA_P0
ADC_DATA_N0
ADC_DATA_P1
ADC_DATA_N1
ADC_DATA_P2
ADC_DATA_N2
ADC_DATA_P3
ADC_DATA_N3
ADC_FCO_P
ADC_FCO_N
ADC_DCO_P
ADC_DCO_N
IC21
CMS
AD9229BCP
P32
PICO
D08
ADC_CLK
50 OHMS
SOT
74anclgu04
INVERSEURS GARDES
PAR PRECAUTION
TBD NPC
SCA_WCK_P
SCA_WCK_N
SCA_RCK_P
SCA_RCK_N
65lvds104
SOIC
CLKW3_P
CLKW3_N
CLKW2_P
CLKW2_N
CLKW1_P
CLKW1_N
CLKW0_P
CLKW0_N
CLKR3_P
CLKR3_N
CLKR2_P
CLKR2_N
CLKR1_P
CLKR1_N
CLKR0_P
CLKR0_N
ROUTER LES
PISTES A
LA MEME
LONGUEUR
P41
PICO
D08
CREATION
14/3/06
X. DE LA BROISE
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
PROJET: TPC T2K - SYSTEME ACQ
ENSEMBLE: CARTE FRONTALE
SOUS/ENS: ADC & TRANS. HORLOGES
NUMERO CIRCUIT
NUMERO PLANCHE 4/6


P5V
FS1
SMD200
2A
POLYSWITCH_CMS
SMD200-2
L13631B
10UH NPC
REF. FARNELL :
1100137
FEC_ID
TBD NPC
WELWYN
LR2512-R10WF
REF. FARNELL :
1100057
0,1 OHMS
1% 2 W
SOIC
IC1
IC2
ad8638
ds2438
P5
PICO
D08
GEN_OUT
PRES DU
GENERATEUR
PRES DU
DS2438
REG_INH_B
D2
N.B. : DIODE PEUT-ETRE INUTILE
PPAK
LD29150PT33
P3V3
P14
P50
P51
AVX TPSD337K006R0045
330 UF 6.3 V 10%
REF. FARNELL :
1135198
UN PRES DU REGULATEUR
L'AUTRE A L'AUTRE EXTREMITE DE LA CARTE
CREATION
14/3/06
X. DE LA BROISE
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
PROJET: TPC T2K - SYSTEME ACQ
ENSEMBLE: CARTE FRONTALE
SOUS/ENS: ALIM. + CONTROLE
NUMERO CIRCUIT
NUMERO PLANCHE 5/6


P43
PICO
D08
J5
FX2
SC
CON80P
MARQUE : HIROSE
MODELE : FX2-80S-1.27DSL(71)
MM_POL0
MM_POL1
SCA_WCK_N
SCA_WCK_P
SCA_READ
SCA_WRITE
SCA_RCK_N2
SCA_RCK_P2
SCA_MISO0
SCA_MISO1
SCA_MISO2
SCA_MISO3
SCA_CS0
SCA_CS1
SCA_CS2
SCA_CS3
FEC_PR_B
ADC_DTP
MM_ID
ADC_PDWN_B
ADC_DCO_P
ADC_DCO_N2
ADC_FCO_P
ADC_FCO_N
ADC_DATA_P0
ADC_DATA_N0
ADC_DATA_P1
ADC_DATA_N1
ADC_DATA_P2
ADC_DATA_N2
SPI_SCLK
SPI_MOSI
ADC_CLK
GEN_OUT
GEN_MISO
GEN_CS
GEN_GO
FEC_ID
RES_S0
REG_INH_B
RES_S1
P28
PICO
D08
SCA-READ
PICO
D08
SCA_READ
SCA-WRITE
PICO
D08
SCA_WRITE
MM-POL0
PICO
D08
MM_POL0
MM-POL1
PICO
D08
MM_POL1
RES-S1
PICO
D08
RES_S1
RES-S0
PICO
D08
RES_S0
J6
PHOENIX_IC25
SC
CON4P
P5V
MARQUE : PHOENIX
MODELE : IC 2,5/ 4-G-5,08
REFERENCE : 1786420
P10
PICO
D08
MIRE_CMS
MIRES CMS
P2
TROUMECA
D0300
P11
TROUMECA
D0300
P3
P12
P4
P16
P5
P17
P7
P19
P6
P22
P8
P23
P20
P21
D0510
P24
D0510
15 TROUS DE 3 MM
PASTILLES DE 7 MM
2 TROUS CENTRAUX
DE POSITIONNEMENT
DE 5,1 MM FINI
PASTILLES DE 8 MM
TROUS POUR FIXATION
DU BLINDAGE
CREATION
14/3/06
X. DE LA BROISE
MODIFICATIONS
DATE
DESSINE PAR
CEA DAPNIA/SEDI
(IL N'EST PERMIS D'UTILISER CE DESSIN QU'AVEC LICENSE SPECIALE (LOI DU 11/3/1957))
PROJET: TPC T2K - SYSTEME ACQ
NUMERO CIRCUIT
ENSEMBLE: CARTE FRONTALE
SOUS/ENS: CONNECTEURS DE SORTIE
NUMERO PLANCHE 6/6


1.1 V
VDD_P
PLAN D'ALIMENTATION SPECIAL POUR LES BLOCS DE PROTECTION
PLACER A GAUCHE DU BLOC DE DIODES
PLACER A DROITE DU BLOC DE DIODES
B_PROT
IN OUT
VDP GP
GND_P\I
CHANGEMENT VALEUR POINT DE RESISTANCES 27/6/07 X. DE LA BROISE
CREATION 14/3/06 X. DE LA BROISE
MODIFICATIONS DATE DESSINE PAR
CEA DAPNIA/SEDI
PROJET: TPC T2K - SYSTEME ACQ
ENSEMBLE: CARTE FRONTALE
SOUS/ENS: BLOC ASIC ; PROTECTION
NUMERO CIRCUIT
NUMERO PLANCHE A1/2


ATTENTION :
LE ROUTAGE DES 4 ASIC
DOIT ETRE STRICTEMENT
IDENTIQUE
(PARTICULIEREMENT
LES CAPACITES 4.7 PF
SUR LA BROCHE IN_CAL)
LQFP
VDD_PROIND
VDD_CSAD2
CIPOL_CSAD
VDD_CSAG2
VDD_PROING
CIPOL_CSAG
VO_N\I
VO_P\I
WRITE\I
50 OHMS
WCK_P\I
WCK_N\I
100 OHMS
RCK_P\I
RCK_N\I
100 OHMS
READ\I
50 OHMS
SC_DOUT\I
SC_CK\I
SC_EN\I
SC_DIN\I
PICO D08
PICO D08
TF\I
CAL\I
MASSE ENTRE PISTES PRES ASIC
CONTROLER LES VALEURS DES RESISTANCES
DECOUPLAGE AU PLUS PRES DES BROCHES
CREATION 14/3/06 X. DE LA BROISE
MODIFICATIONS DATE DESSINE PAR
CEA DAPNIA/SEDI
PROJET: TPC T2K - SYSTEME ACQ
ENSEMBLE: CARTE FRONTALE
SOUS/ENS: BLOC ASIC ; ASIC
NUMERO CIRCUIT
NUMERO PLANCHE A2/2



CREATION	14/3/06	X. DE LA BROISE
MODIFICATIONS	DATE	DESSINE PAR

CEA DAPNIA/SEDI

PROJET: TPC T2K - SYSTEME ACQ	NUMERO CIRCUIT
ENSEMBLE: CARTE FRONTALE	
SOUS/ENS: BLOC PROTECTION	NUMERO PLANCHE B1/1

6.4 Nomenclature.

Here is the list of the 1302 components to cable and the 75 components not to cable (NPC).

Components to cable

Part Name	Référence	JEDEC_TYPE	Ref Des	VALUE	VOLT	TOL	Qty
74AHC1GU04_SOT-BASE	74AHC1GU04 (réf. Farnell 1287411)	SOT23-5	IC17,IC18	?	?	?	2
74HC595_SOIC-4	74HC595 (réf. Farnell : 9591656)	SO_16	IC12,IC16	?	?	?	2
74LVC125_SOIC-BASE	74LVC125 (réf. Farnell : 1236303)	SO_14	CI1	?	?	?	1
AD1580_SOT-BASE	A.D., AD1580BRTZ-REEL7	TO236	IC15	?	?	?	1
AD8041_SO-BASE	A.D., AD8041ARZ	SO_8	IC11	?	?	?	1
AD8628_SOIC-BASE	A.D., AD8628ARZ	SO_8	IC1	?	?	?	1
AD9229BCP_CMS-BASE	A.D., AD9229BCPZ-50	LFCSP49	IC21	?	?	?	1
AD9744_TSSOP-BASE	A.D., AD9744ARUZ	TSSOP28	IC14	?	?	?	1
AFTER_LQFP-BASE		LQFP160	CI4,CI6,CI8,CI10	?	?	?	4
BAV99_SOT-BASE		SOT323 (BAV99W)	D1,D3,D5,D6,D7,D8,D9,D10,D11,D12,D13,D14,D15,D16,D17,D18,D19,D20,D21,D22,D23,D24,D25,D26,D27,D28,D29,D30,D31,D32,D33,D34,D35,D36,D37,D38,D39,D40,D41,D42,D43,D44,D45,D46,D47,D48,D49,D50,D51,D52,D53,D54,D55,D56,D57,D58,D59,D60,D61,D62,D63,D64,D65,D66,D67,D6	?	?	?	288
CCER-100N13		603	C3,C4,C22,C24,C25,C26,C27,C28,C29,C30,C32,C33,C34,C35,C36,C37,C38,C40,C41,C42,C44,C45,C47,C48,C49,C50,C51,C52,C53,C56,C57,C58,C59,C60,C65,C67,C73,C75,C76,C77,C78,C79,C80,C82,C85,C87,C88,C89,C90,C91,C92,C93,C95,C96,C97,C98,C99,C100,C101,C103,C104,C105,C106	100nf	16V	10%	179
CCER-10N9		603	C6,C84,C134,C183,C233	10nf	63V	20%	5
CCER-10U4		1206	C8,C9,C10,C12,C13,C14,C15,C16,C17,C18,C20,C21,C23,C31,C39,C46,C54,C66,C74,C83,C86,C94,C102,C108,C115,C123,C127,C132,C136,C144,C152,C158,C165,C173,C182,C185,C193,C201,C207,C214,C223,C227,C232,C327,C361,C384,C395,C479,C481,C482,C483,C484	10uf	16V	10%	52
CCER-10U7		1210	C476	10uf	25V	10%	1
CCER-220P11	Kemet, C0805C221JCRAC7800	805	C234,C235,C236,C237,C238,C239,C240,C241,C242,C243,C244,C245,C246,C247,C248,C249,C250,C251,C252,C253,C254,C255,C256,C257,C258,C259,C260,C261,C262,C263,C264,C265,C266,C267,C268,C269,C270,C271,C272,C273,C274,C275,C276,C277,C278,C279,C280,C281,C282,C283,C284,	220pf	500V	5%	288
CCER-220P7		603	C43	220pf	50V	5%	1
CCER-22U4		1206	C81,C131,C180,C230	22uf	10V	20%	4
CCER-330N4		805	C7	330nf	50V	10%	1
CCER-4P75	0603 4,7 pF 0,7 % (réf. Farnell : 8819793)	603	C2,C19,C69,C219	4.7pf	50V	0,70%	4
CCER-4U72		1206	C5	4.7uf	63V	20%	1
CON4P_PHOENIX_IC25-18	(réf. RS : 292-9206)	IC25_4G508	J6	?	?	?	1
CON80P_FX2-SC	Hirose, FX2-80S-1.27DSL(71)	FX2_80S_127 DSL	J5	?	?	?	1
CON80P_SMC114806-PC	Erni, SMCB 80 M AB VV 3-03, référence 114806	SMC114806	J1,J2,J3,J4	?	?	?	4
CPOL-100U17	(réf. Farnell : 1135233)	S35X28POL	C133	100uf	6.3V	20%	1
CPOL-10U22		1206POL	C11	10uf	20V	10%	1
CPOL-330U4	(réf. Farnell : 1135198)	S73X43POL	C551,C552	330uf	6.3V	10%	2
DS2438_SOIC-BASE	Maxim Dallas, DS2438az+	SO_8	IC2	?	?	?	1
FUSE2P-2A7	SMD200-2 (réf. RS 517-7082)	SMD200	FS1	2A	?	?	1
LD29150_PPAK-BASE	STM, LD29150PT33	PPAK	RG2	?	?	?	1
LED_SMD_LSA670-27	(réf. RS : 654-4146)	A670	D4	?	?	?	1
LP2951_SOIC-3	National Semiconductor, LP2951ACD-3.3G	SO_8	IC26	?	?	?	1
PLA143_SO-BASE	PLA143S	SO_6	CI2,CI3	?	?	?	2

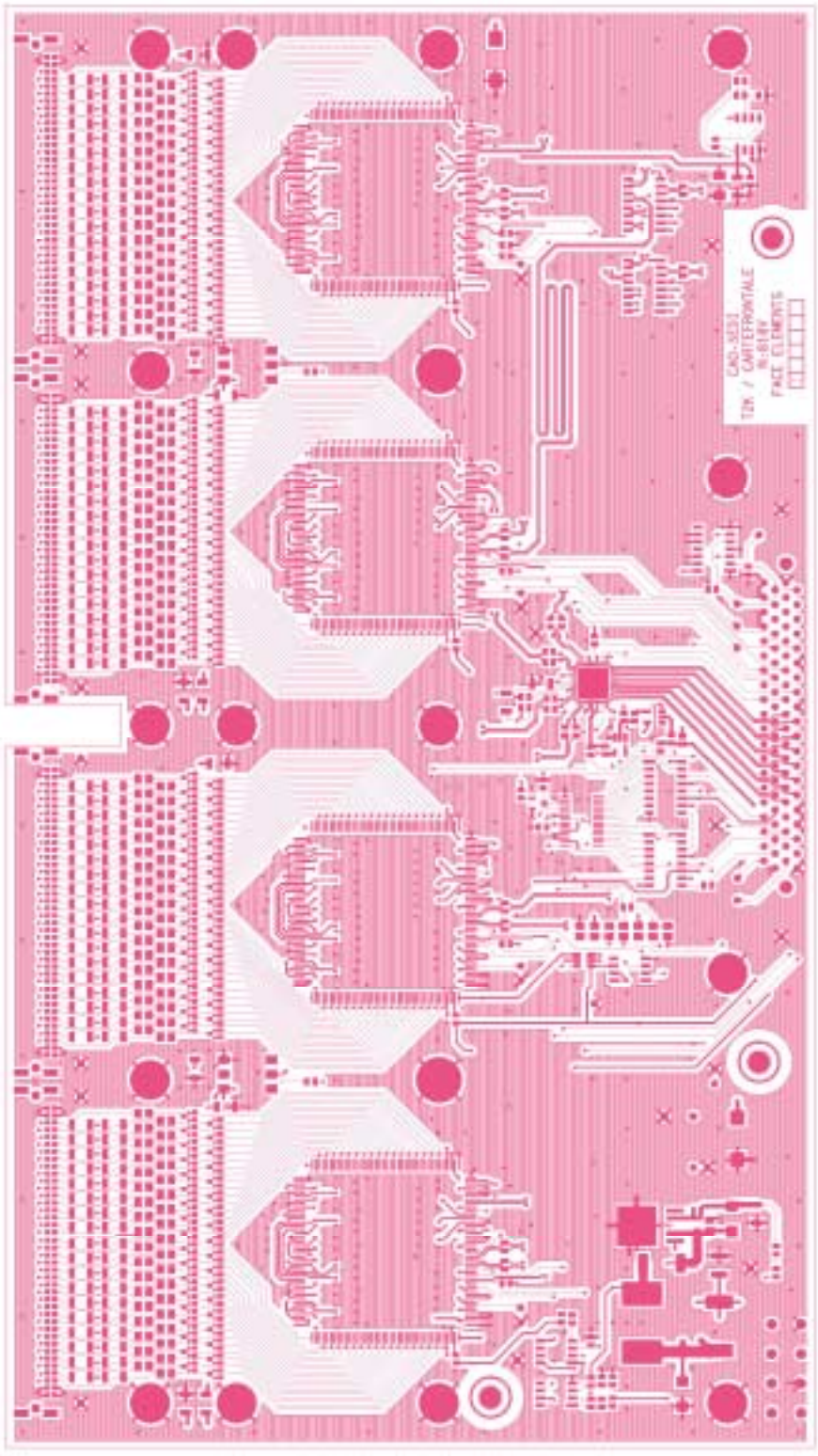
RES0603-0		603	R7,R9,R25,R30,R34,R36,R41,R45,R58,R67,R71,R73,R77,R81,R88,R94,R106,R108,R113,R117,R119,R129,R134,R146,R151,R155,R157,R161,R165	0	?	5%	29
RES0603-1.24K		603	R31,R68,R114,R152	1.24k	?	5%	4
RES0603-10		603	R54,R93,R143,R174	10	?	5%	4
RES0603-100		603	R37,R51,R52,R53,R91,R92,R141,R142,R172,R173,R225,R246	100	?	5%	12
RES0603-100K		603	R6,R179,R184	100K	?	5%	3
RES0603-100K		603	R2,R4	100K	?	1%	2
RES0603-10K		603	R15,R18,R19,R20,R21,R22,R23,R40,R42,R83,R132,R298	10K	?	5%	12
RES0603-17.4k		603	R3	17.4k	?	5%	1
RES0603-2.1K		603	R39,R44,R75,R80,R123,R133,R159,R164	2.1k	?	1%	8
RES0603-200K		603	R1,R5	200K	?	1%	2
RES0603-2K		603	R35,R72,R85,R118,R156	2K	?	5%	5
RES0603-3.32K		603	R32,R69,R115,R153	3.32k	?	1%	4
RES0603-3.92K		603	R27,R60,R110,R148	3.92k	?	1%	4
RES0603-33		603	R95,R96,R98,R99,R124,R125,R126,R127	33	?	5%	8
RES0603-4.99K		603	R47,R48,R84,R86,R136,R137,R167,R168	4.99k	?	1%	8
RES0603-470		603	R8,R10,R14	470	?	5%	3
RES0603-4K		603	R107	4K	?	5%	1
RES0603-5.1K		603	R11,R26,R29,R59,R66,R109,R112,R147,R150	5.1K	?	5%	9
RES0603-6.04K		603	R28,R65,R111,R149	6.04k	?	1%	4
RES0603-6.65K		603	R33,R70,R116,R154	6.65k	?	1%	4
RES0603-7.87K		603	R38,R43,R74,R79,R122,R131,R158,R163	7.87k	?	1%	8
RES0805-1.02K		805	R61,R62	1.02k	?	0.1%	2
RES0805-226		805	R63,R64	226	?	0.1%	2
RES0805-24.9		805	R287,R296	24.9	?	0.1%	2
RES0805-510		805	R56	510	?	0.1%	1
RES0805-6.34K		805	R282	6.34k	?	0,10%	1
RES1206-0		1206	R49,R50	0	?	1%	2
RES1206-100M	SRT, CHS 1206 NA 100M 20% 600V	1206	R176,R177,R178,R180,R181,R182,R183,R185,R186,R187,R188,R190,R191,R192,R193,R194,R195,R196,R197,R198,R199,R200,R201,R202,R203,R204,R205,R206,R207,R208,R209,R210,R211,R212,R213,R214,R215,R216,R217,R218,R219,R220,R221,R222,R223,R224,R226,R227,R228,R229,R230,	100M	600V	20%	288
RES1206-1M		1206	R24,R57,R101,R145	1M	?	1%	4
RES1206-3.3M		1206	R12,R13,R16,R17	3.3M	?	1%	4
RES2512-0.1	(réf. Farnell : 1100067)	S63X31_2512	R46	0.1	?	1%	1
S2A_DO-BASE	Diode S2A (réf. Farnell : 7277954)	DO214AA	D2,D149	?	?	?	2
SN65LVDS104_SOIC-BASE	Texas Instrument, SN65LVDS104D	SO_16	IC28,IC29	?	?	?	2
TS5A3159_SOT-BASE	TS5A3159 (réf. Farnell : 1053237)	SOT23-6	SW1	?	?	?	1
TOTAL							1302

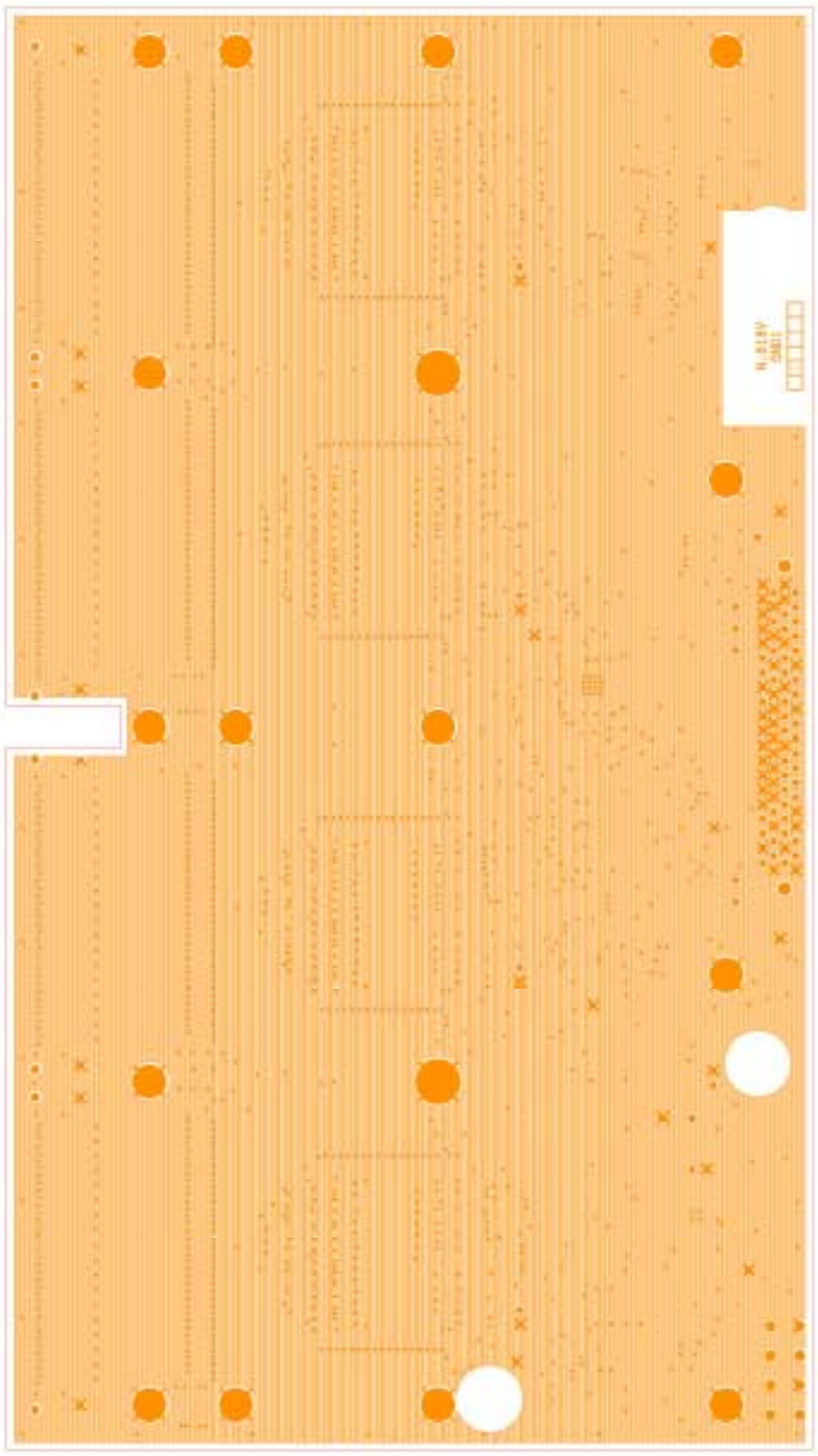
Components not to cable (NPC)

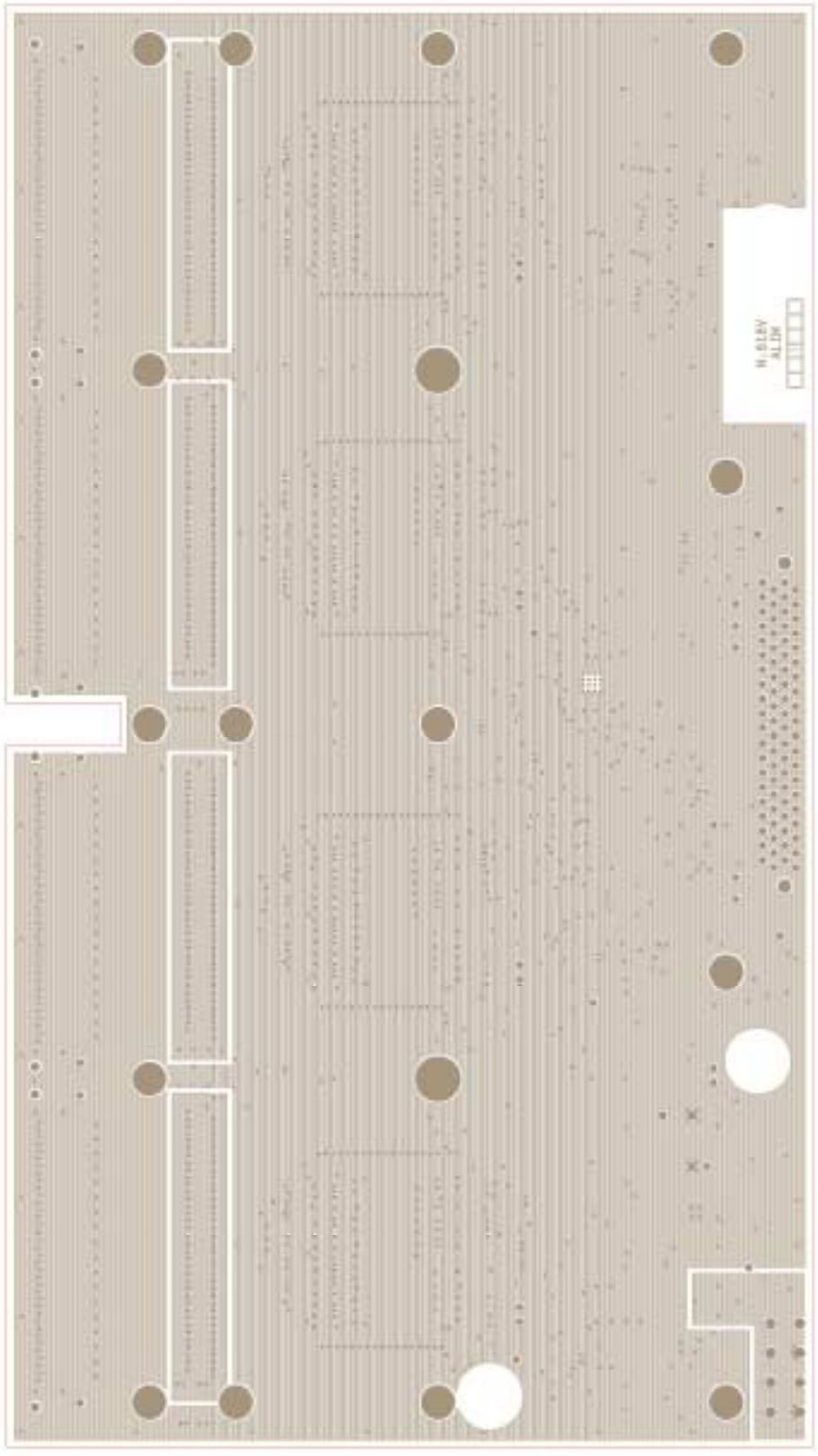
Part Name		JEDEC_TYPE	Ref Des	VALUE	VOLT	TOL	Qty
CCER-1P5		603	C1,C55,C61,C62,C63,C64,C68,C70,C71,C72,C478	1pf	50V	5%	11
CPOL-1000U2		RAD125	C130	1000uf	25V	20%	1
RES0603-0		603	R100,R105,R189	0	?	5%	3
RES0603-50		603	R102	50	?	5%	1
RES0603-TBD		603	R103,R104,R120,R121	TBD	?	5%	4
SELF-10U4		3631B	L1	10uH	?	?	1
MIRE_CMS_TYPE_1-BASE		MIRE_CMS_1	MIR1,MIR2,MIR3	?	?	?	3
PICO_PICO-2		PINDIA08	3V3,MM-POL0,MM-POL1,P1,P6,P10,P14,P15,P18,P25,P26,P27,P28,P29,P30,P31,P32,P33,P34,P36,P38,P39,P41,P43,P44,P45,P47,P50,P51,P52,RES-S0,RES-S1,SCA-READ,SCA-WRITE	?	?	?	34
TROUMECA_TROUMECA-22		M300	P2,P3,P4,P5,P7,P8,P9,P11,P12,P16,P17,P19,P20,P22,P23	?	?	?	15
TROUMECA_TROUMECA-59		M510	P21,P24	?	?	?	2
TOTAL							75

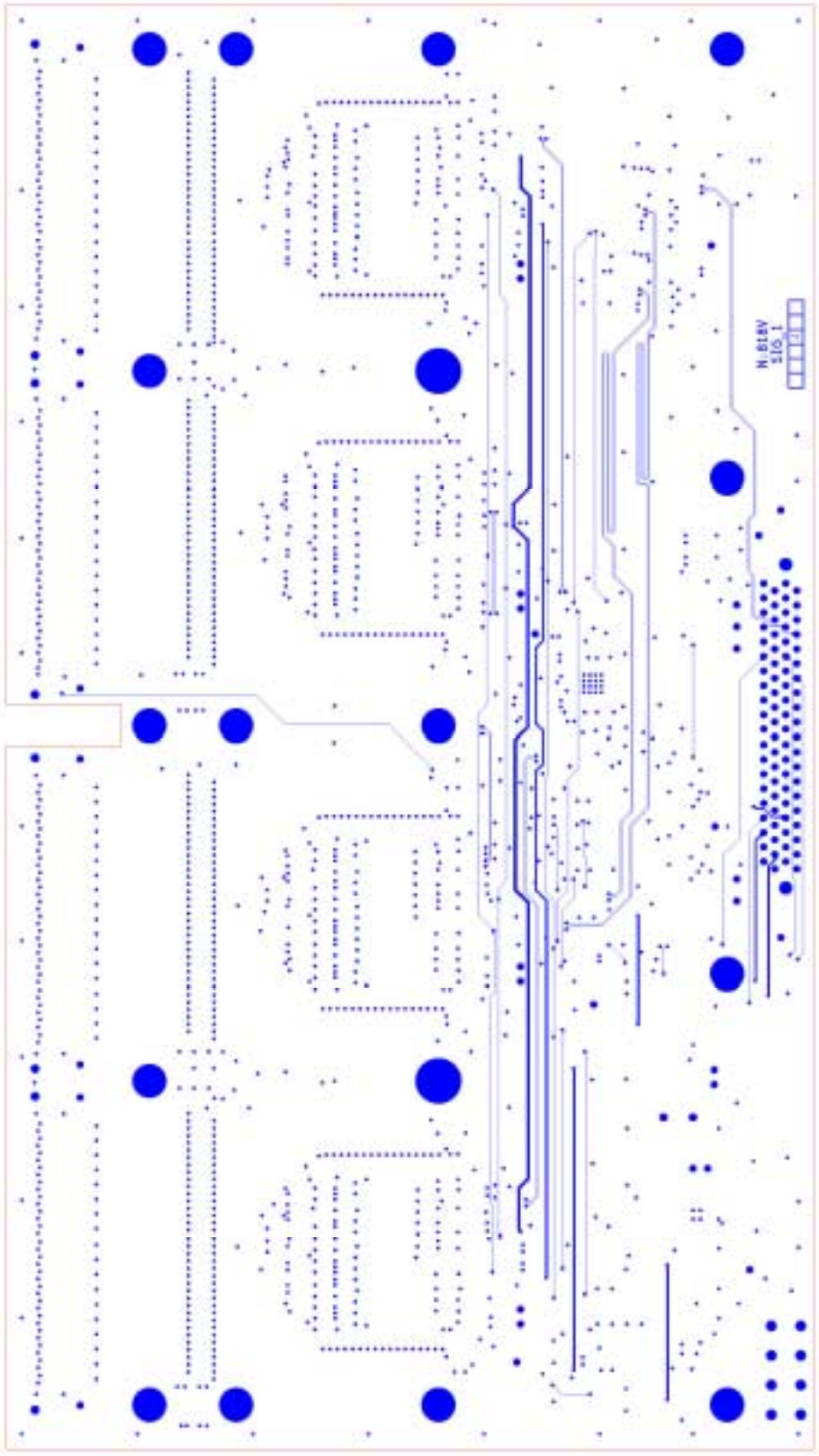
7 Routing layout (PCB).

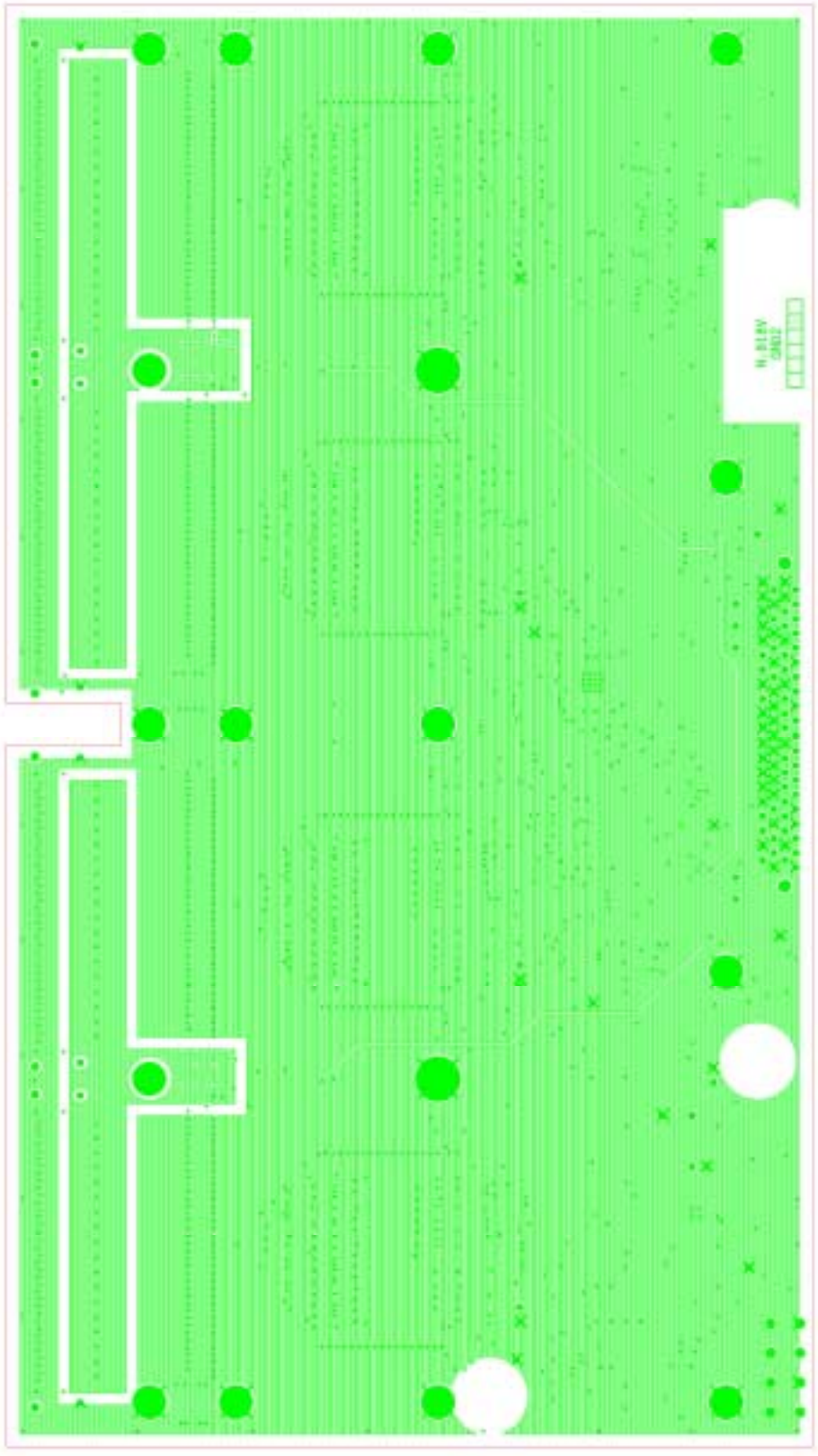
This section gives the routing the six layers of the printed circuit.

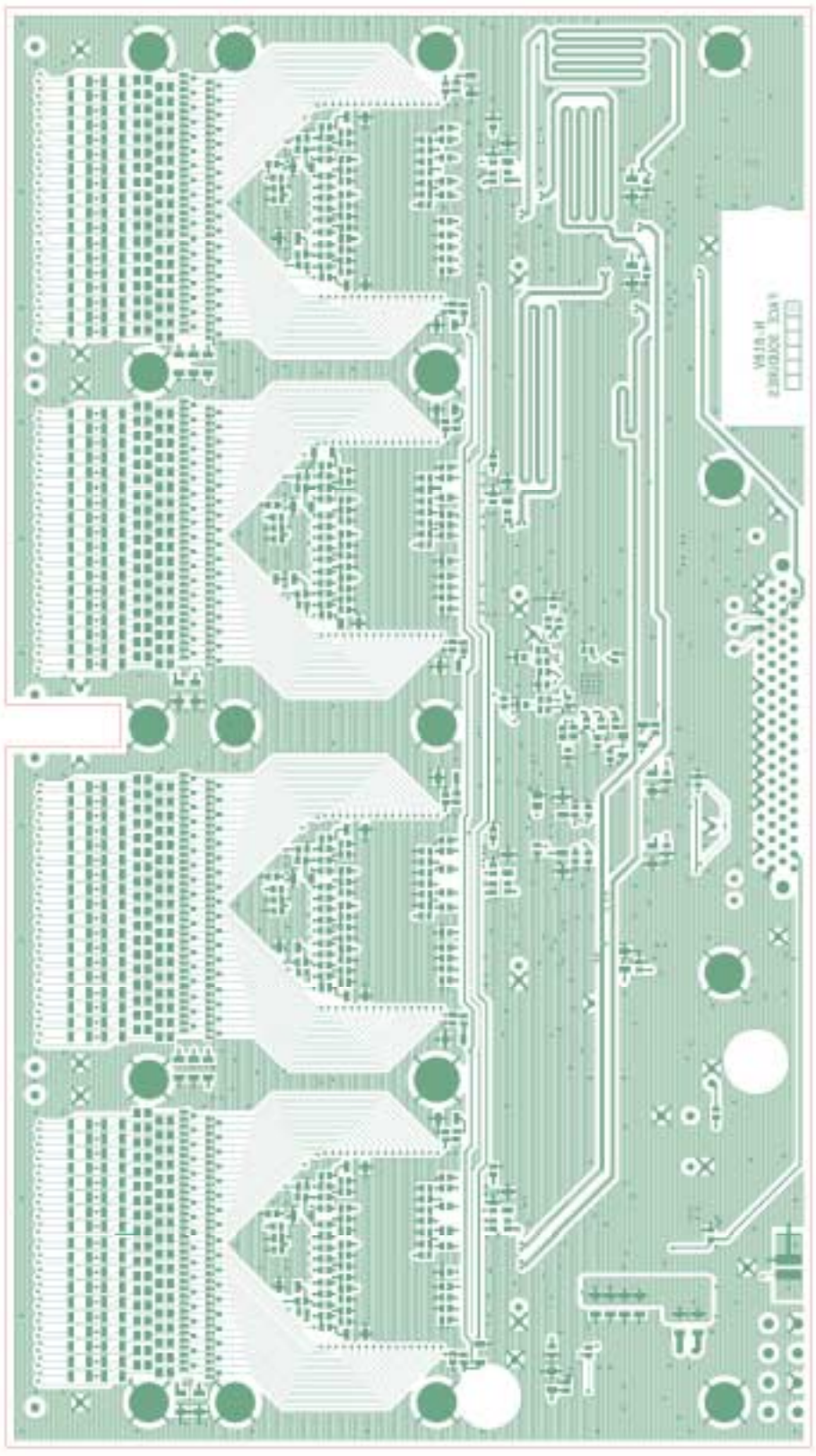


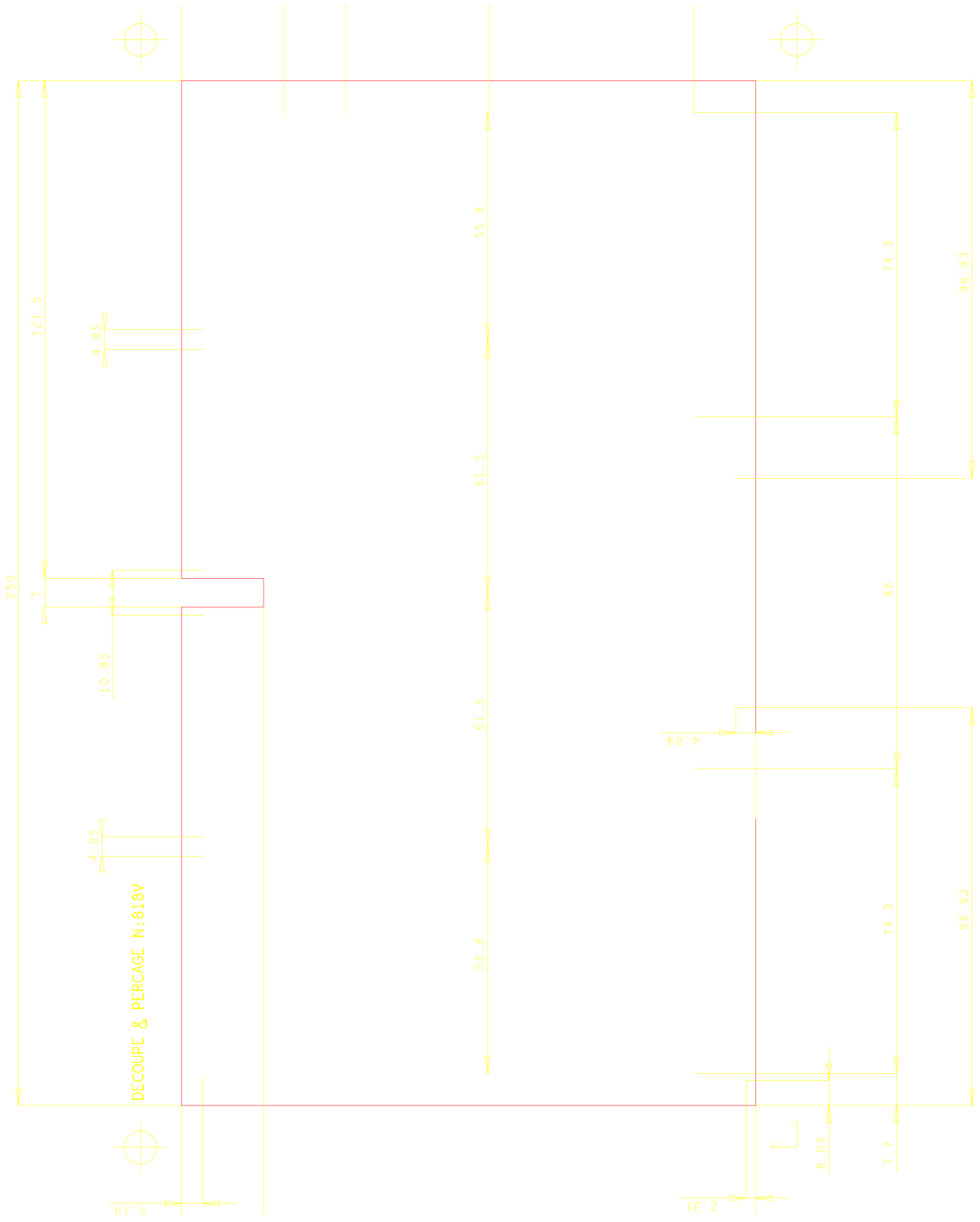











DECOUPE & PERCAGE N:818V
250
121.5
4.85
7
10.85
4.85
55.8
61.5
61.5
55.8
74.3
96.93
86
4.89
74.3
96.93
6.04
7.7
2.31

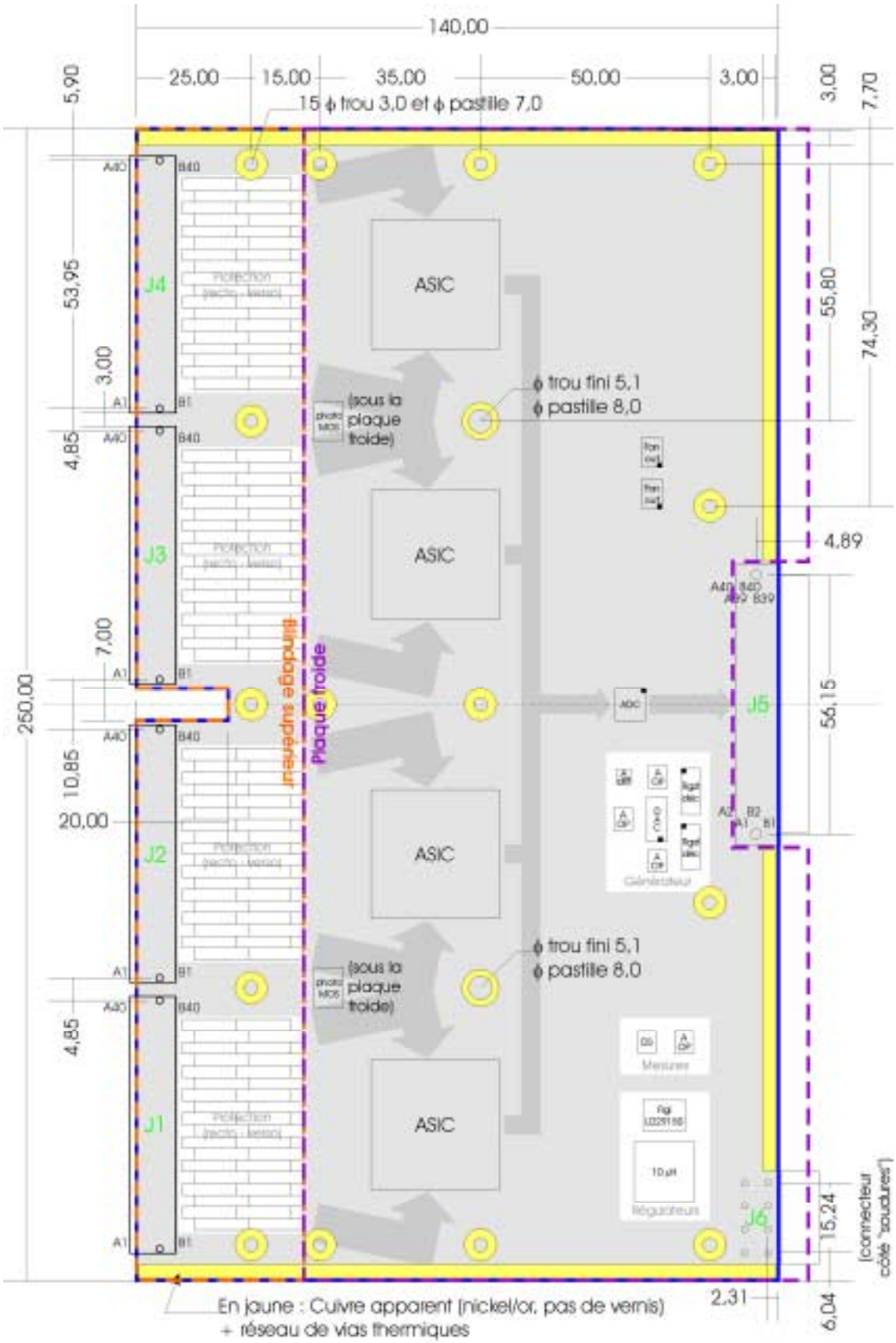
8 Mechanical layout.

8.1 Printed circuit outline.

The layout of the outline of the board, of the position of the fixation holes and of the connectors is given bellow (both side). Two holes, in central position, have a bigger diameter than others. They are used to centre the cooling plates according to the board.

The Bands (yellow) around the board where the copper is not varnished is designed to make a good electromagnetic contact between the cooling and shielding plates and the board. Along these bands, a succession of vias connected to the PCB ground plans completes the shielding.

A notch has been designed between the two central input connectors to leave place for the mechanical structure of the Micromegas detector.


140,00
25,00
15,00
35,00
50,00
3,00
3,00
7,70
5,90
15 ϕ trou 3,0 et ϕ pastille 7,0
ASIC
ASIC
ASIC
ASIC
J4
J3
J2
J1
J5
J6
53,95
3,00
4,85
7,00
10,85
20,00
4,85
250,00
55,80
74,30
4,89
56,15
15,24
2,31
6,04
ϕ trou fini 5,1
ϕ pastille 8,0
(sous la plaque froide)
ϕ trou fini 5,1
ϕ pastille 8,0
(sous la plaque froide)
Plaque froide
Embase supérieure
(connecteur côté "soudures")
En jaune : Cuivre apparent (nickel/or, pas de vernis)
+ réseau de vias thermiques


3,00
3,00
7,00
blindage intérieur froid
J6
2,50
En jaune : Cuivre apparent (nickel/or, pas de vernis)
+ réseau de vias thermiques

8.2 Cooling and shielding plates.

A picture of the assembling of the cooling and shielding plates, and a layout (for top and bottom sides of the board) are given bellow.

- Plate for the top side of the board.

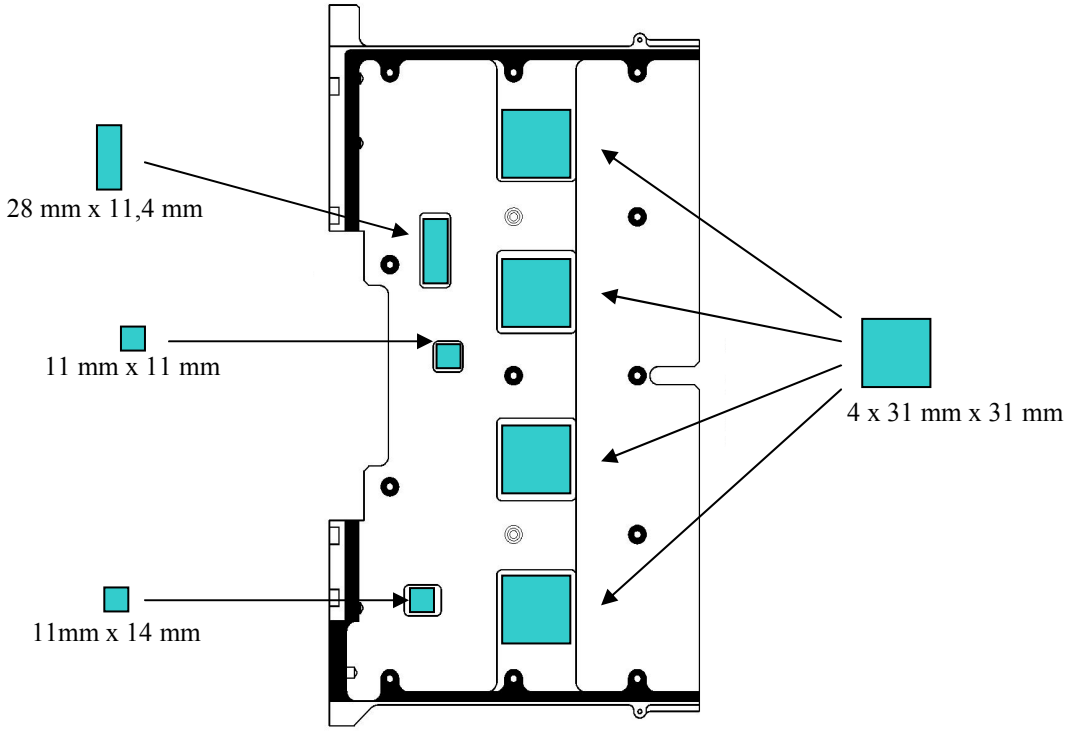
Almost all the active components of the board have been collected on this side of the board. So the top side plate is specifically designed to cool them. In addition, it shields the board. Among these hot components, eight dissipate more than the others :

- the regulator LD29150,
- the four After ASIC,
- the ADC AD9229,
- and the two LVDS repeaters 65LVDS104.

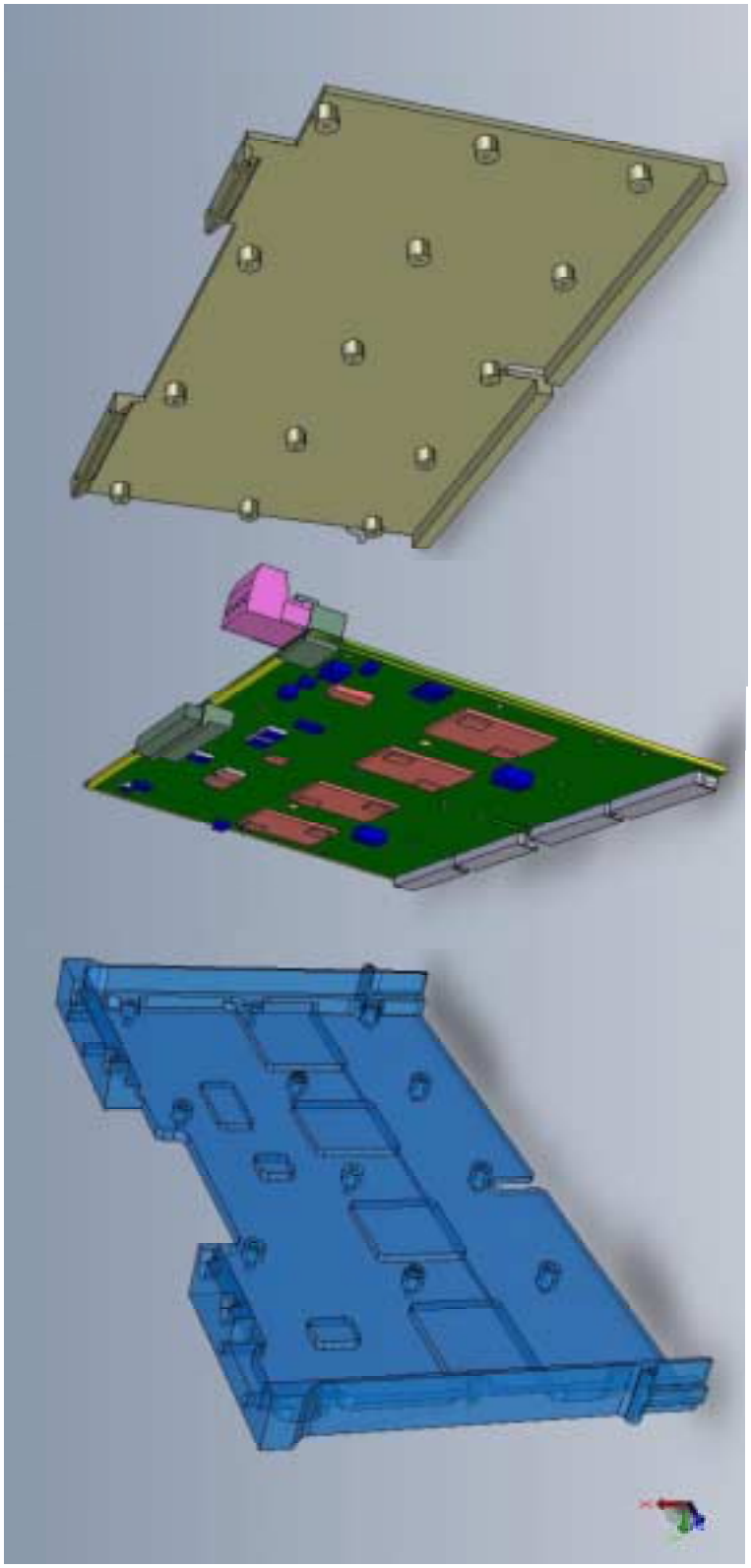
It is the reason why these components are specifically cooled : seven zones of the plate have been designed so that their surface is nearer of the top of these components, and a self-adhesive thermal moss (depth : 1 mm) makes the contact between the component package and the plate. The position of these zones are showed just bellow.

- Plate for the bottom side of the board.

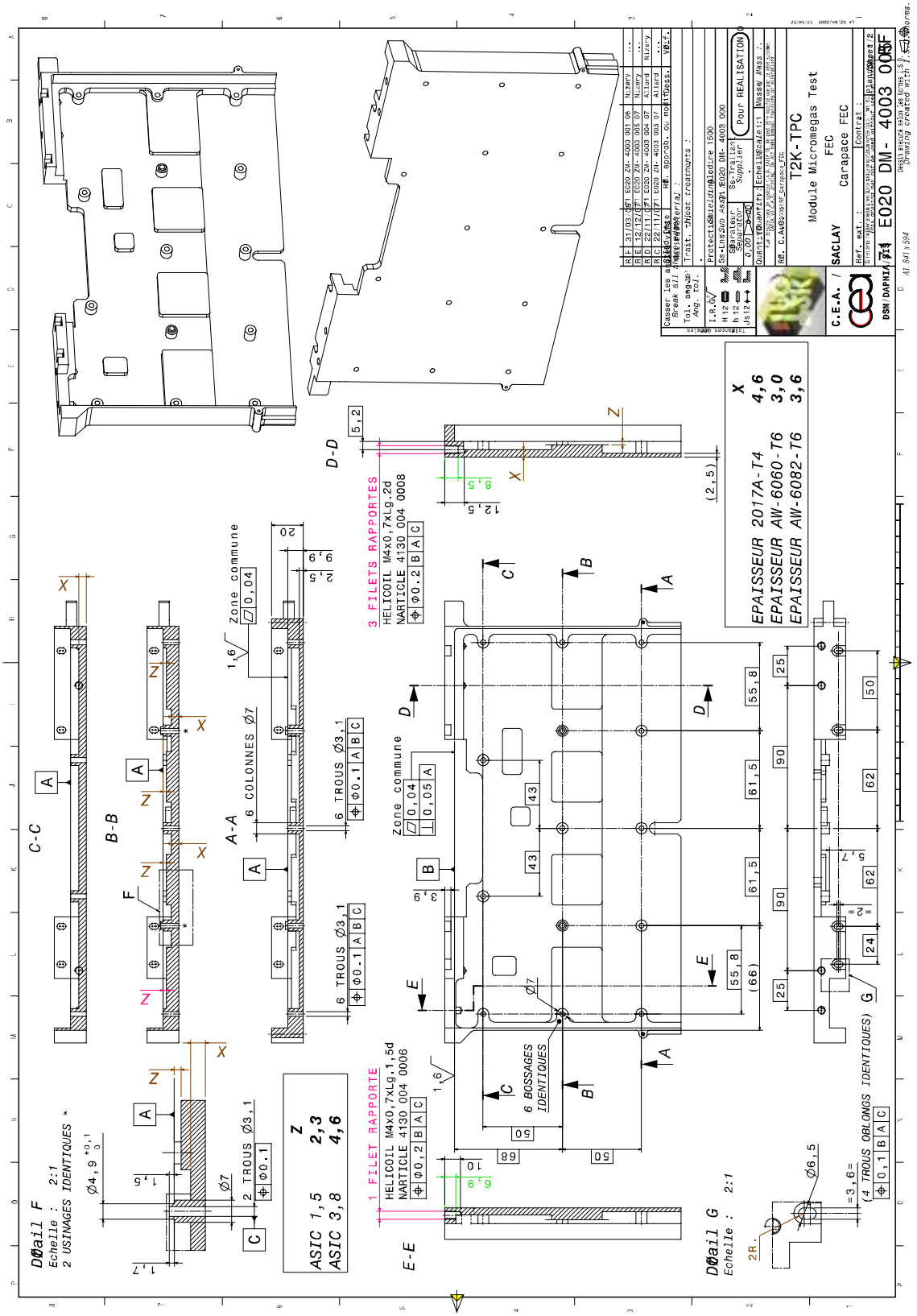
The dissipation at the bottom side of the board is almost zero. So the aim of this second plate is firstly to electromagnetically shield the board, and secondly to remove the calories at the level of the four input connectors and to guide them to the cold source. This avoids that the electronics heat up the detector and so the gas of the TPC, which would create convection movements that could perturb its performance. This cooling could not be done by the other cooling plate, because its hot shots created by the hot components act like barrier for the calories coming from the connectors to the cold source.



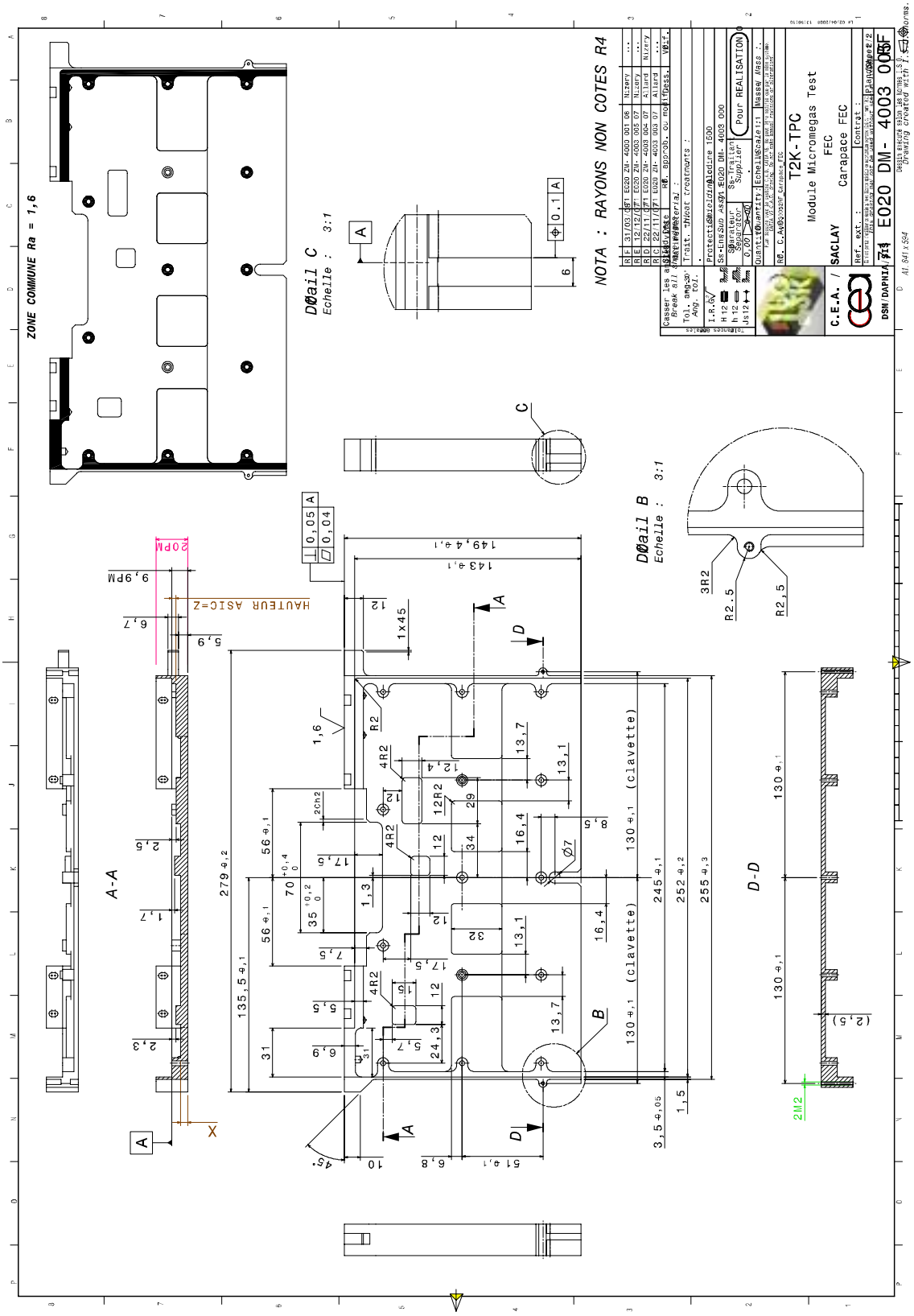
Position of the thermal mosses (in blue) on the top side plate.



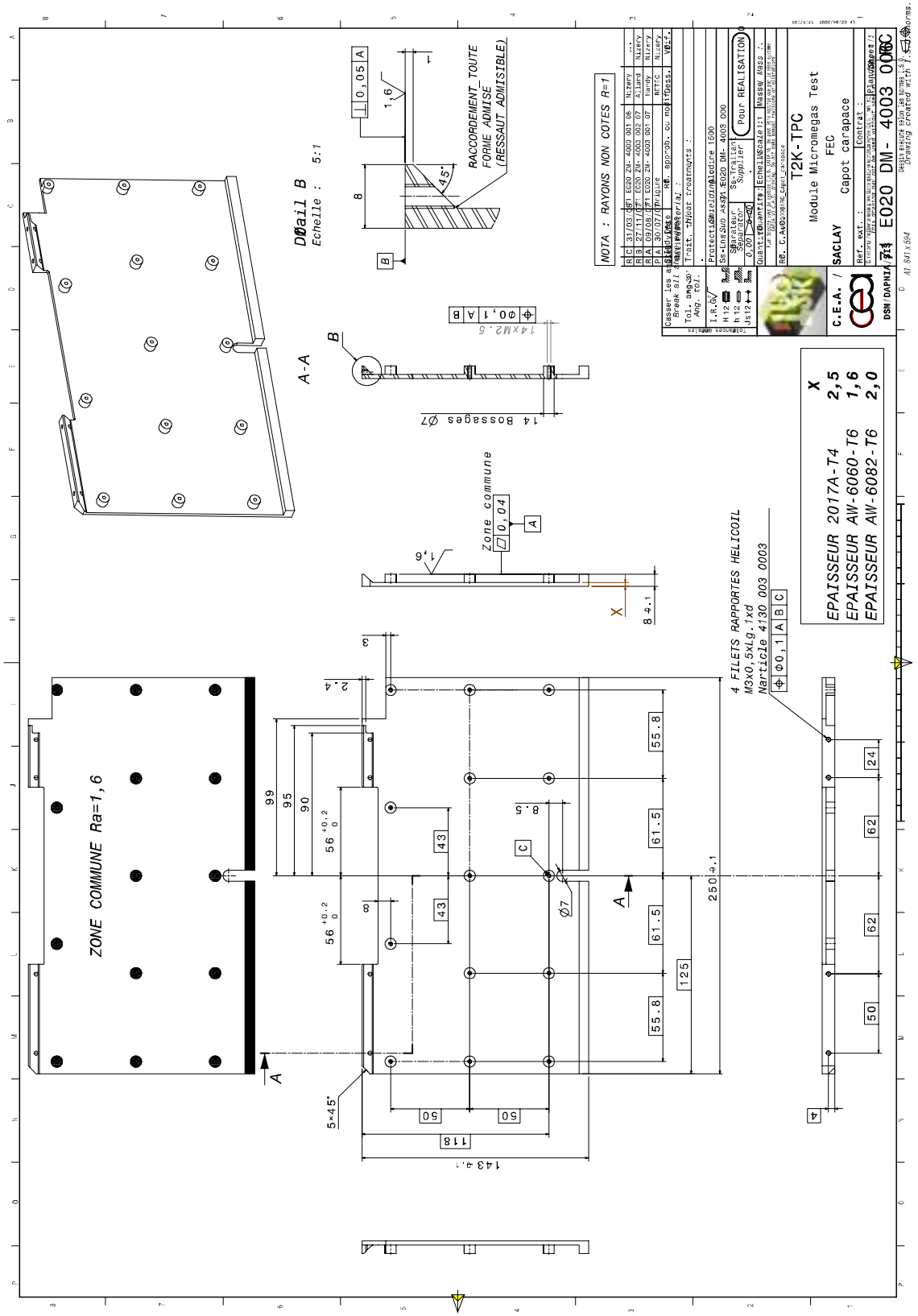
Assembling of the two shielding plates on the FEC board



Shielding plate for the top side of the board (1/2)



Shielding plate for the top side of the board (2/2)



Shielding plate for the bottom side of the board