TPC Electronics

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FEC Design

- Our Requirements:
  - 12 bit ADC
  - internal triggering
  - reduced number of buckets to be readout
  - 1kHz event rate
  - board layout must allow for minimum pad spacing (0.5cmx0.5cm)
- Designed & constructed at Saclay

Parameter	Value
Polarity of detector signal	Negative or Positive
Number of channels	72
External Preamplifier	Yes; access to the filter or SCA inputs
Charge measurement	
Input dynamic range	120 fC; 1 pC; 10 pC
Gain	Adjustable/(channel)
Output dynamic range	2V p-p
I.N.L	< 2%
Resolution	< 850 e- (Charge range: 120fC; Peaking Time: 200ns; Cinchannel. < 30pF)
Sampling	
Peaking time value	50 ns to 1 µs (16 values)
Number of SCA Time bins	511
Sampling Frequency	1 MHz to 100 MHz
Time resolution	
jitter	60 ps rms
skew	< 700 ps rms
Trigger	
Discriminator solution	L.E.D
Trigger Output/Multiplicity	OR of the 72 hit channel registers; Current output
Dynamic range	5% of input charge range
I.N.L	< 5%
Threshold value	4-bit DAC/channel + (3-bit + polarity bit) common DAC
Minimum threshold value	≥ noise
Readout	
Readout frequency	20 MHz to 25 MHz
Channel Readout mode	Hit channel; specific channels; all channel
SCA Readout mode	511 cells; 256 cells; 126 cells
Test	
calibration	1 channel / 72; external test capacitor
test	1 channel / 72; internal test capacitor (1/charge range)
functional	1, few or 76 channels; internal test capacitor/channel
Counting rate	
ASIC level	< 1 kHz
Power consumption	
Channel | Asic	< 10 mW / channel
Packaging	Ceramic or plastic
Temperature	ambient

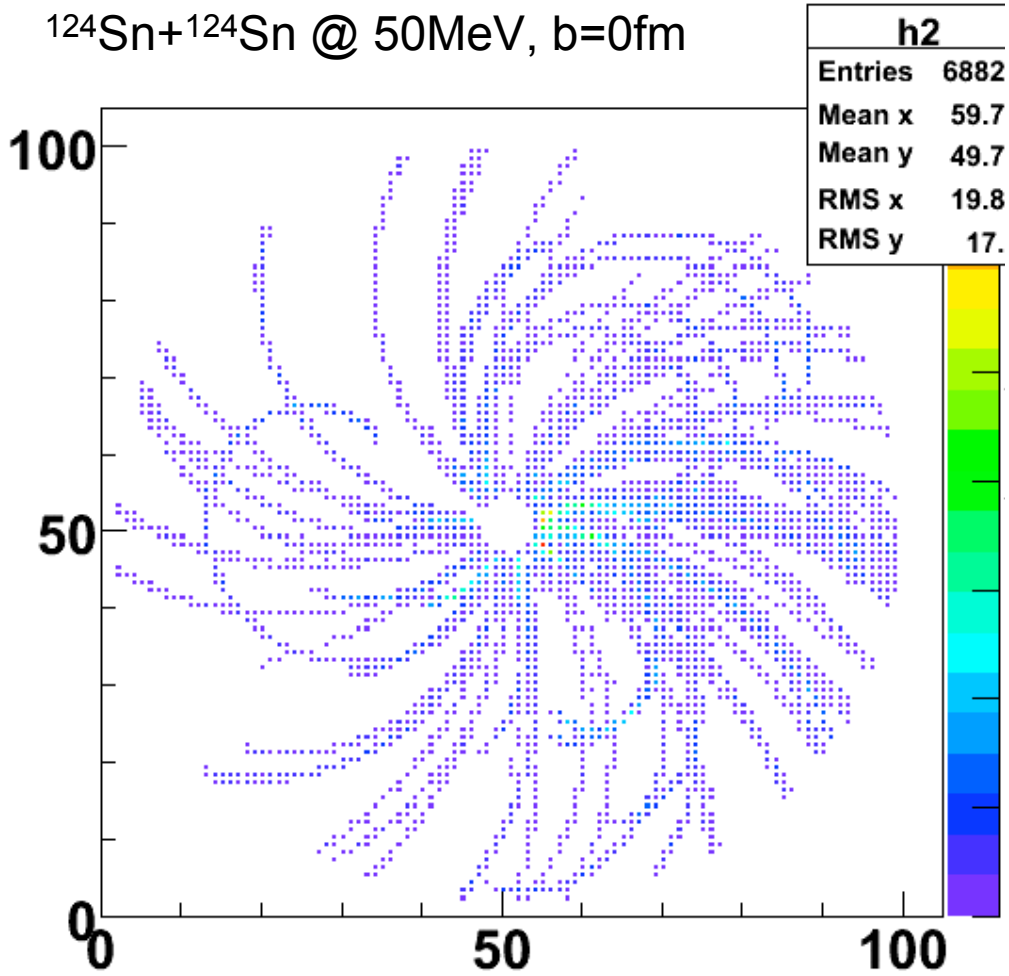
FEC Design

- Our Questions:
  - Where does zero-suppression occur? In the FEM? Prefer early, but must be after trigger decision
  - What are the T2K card dimensions? (14cmx25cmx2cm => where did these numbers come from?)
  - What type of connectors interface with the pad plane?
  - Do After+ requirements in March 28 document match our needs? Have these parameters changed in the past month? (see previous slide)

FEC: Rate Requirements

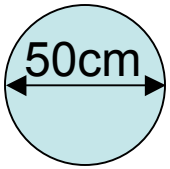
- Required FEC rates:
  - 1kHz trigger rate
  - 43% pad occupancy
  - 0.3% time occupancy (511 bins)
  - 0.7% time occupancy (128 bins)
  - Assumptions
    - 72 chan per ADC
    - 4 ADC per FEC
    - 128 time bins
  - Per event data volume:
    - Assume zero suppressed
      - (72*0.43)*(128*0.01)*4*1000*12 = 2 Mbit/s/FEC
      - Must add additional x10 to account for signal smearing
    - No zero suppression
      - 72*128*4*1000*12 = 440 Mbit/s/FEC

$^{124}Sn+^{124}Sn$ @ 50MeV, b=0fm

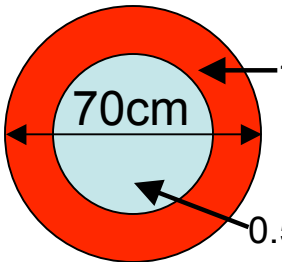


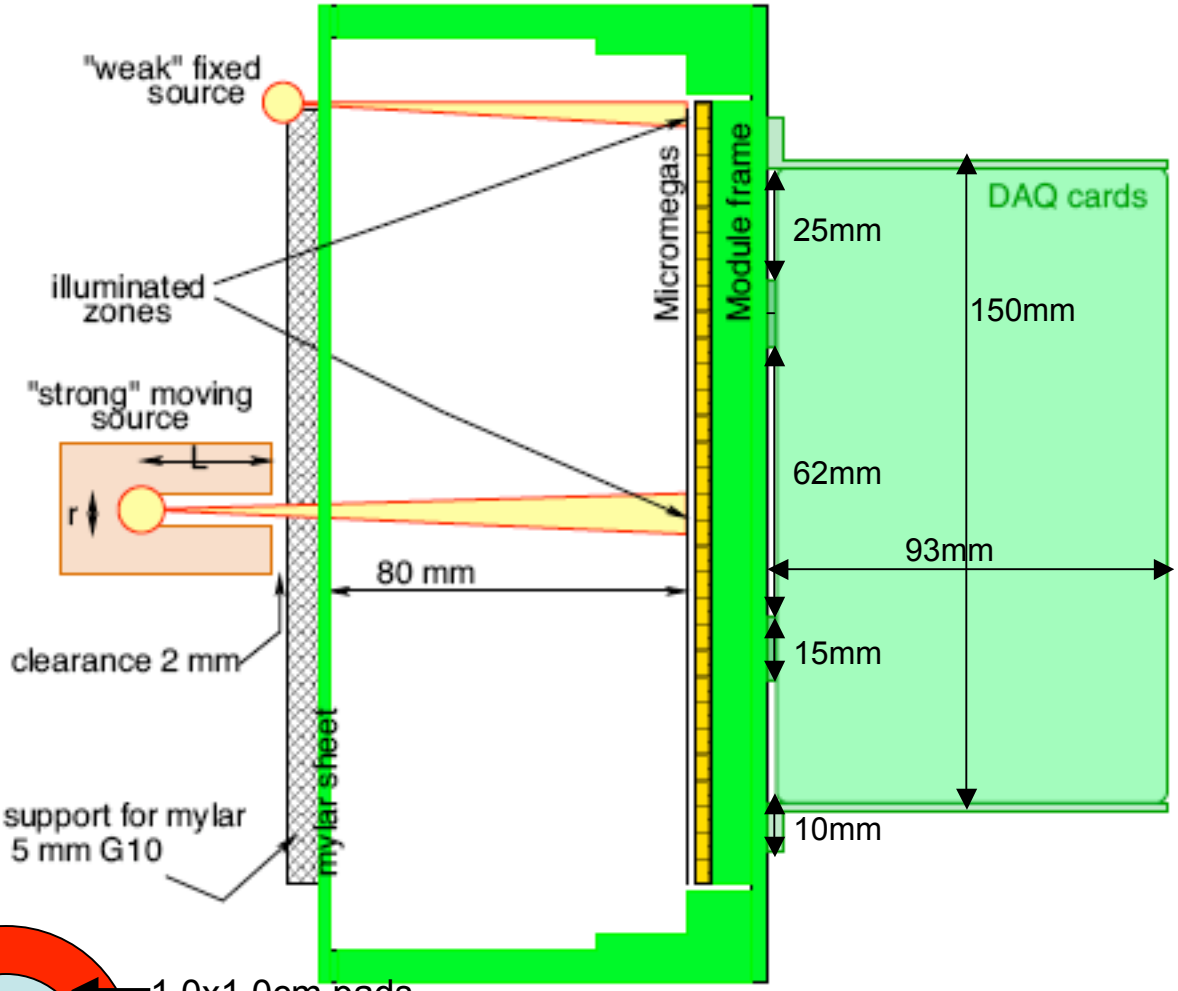
FEC: Physical Constraints

- Geometry
  - Board size
  - Connector size & spacing
- Readout Plane
  - NSF design = 1963cm^2
    - #pads = 7268
    - Pads = 0.5cmx0.5cm
    - Beam window radius = 2cm
    - #FEC = 26
    - Total Data = 52Mbit/s

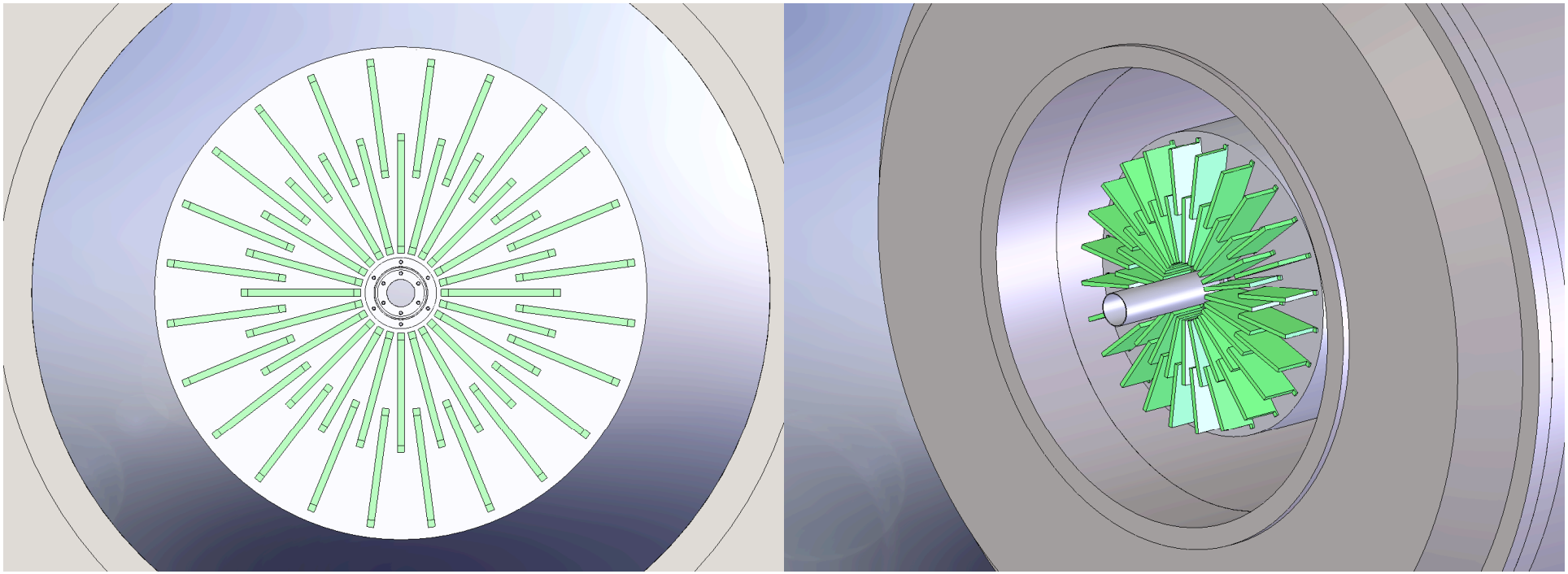


  - TWIST design = 3848cm^2
    - Inner radius = 25cm
    - Outer radius = 35cm
    - #pads = 9739
    - #FEC = 34
    - Total Data = 68Mbit/s





FEC: Physical Constraints



Assume: FEC width = 1cm
TWIST dimensions

Result: 48 cards arranged in groups of 24
minimum separation 7.5mm*
does not allow FEM bridge

FEM: Design Requirements

- Our Requirements:
  - Assume 6 FEC per FEM => 12 Mbit/s
  - #FEM = 6 (TWIST geometry)
- Our Questions:
  - Why can current T2K FEM design not go above a rate of 10Hz? => this appears to be due to the programing of the FPGA.
  - Is data compression or zero suppression occurring during the readout of this memory? => according to the numbers in the FEM Design Notes the estimated max rates are based on empty events => What will be the effect of real data?
  - What functionality is included in FPGA?
  - Issue with FPGA to Memory storage & readout; we would like to achieve 1kHz - need to examine Santiago Meeting slides to understand if proposed modifications are capable of achieving this and if they are the best method?
  - Can we transfer the zero suppression to the FPGA in the FEM?
  - What readout and time stamping scheme do we prefer? (evaluate continuous readout proposal & other options)
  - Define the mechanical connection between the FEC & FEM? Mounting the FEM perpendicular to 6 FEMs limits the geometrical arrangement.
  - If the FEC design remains the same with a modified AFTER+ chip, how far can the signal be sent?
  - 2-3 years required, is this reasonable?
- Bordeaux (Is there sufficient manpower for entire project???

FEM: Physical Constraints

- Consider 3 scenarios
  - 6xFEC per FEM (T2K design)
    - Direct connection btwn boards?
    - Short cable between boards?
  - 1xFEC per FEM
    - Direct connection btwn boards?
    - Short cable between boards?
  - Combine FEC and FEM on same board

DCC

- Our Questions:
  - Why is it necessary, particularly if it only can combine 2FEMs?
  - What is intrinsic rate limitation of commercial design?
  - Is the manufacturer and hardware reliable?
  - What is a realistic estimate of amount of time required to program the card; will this be done as a collaboration or individually?
  - 2-3 years required?
  - Designed & constructed Ganil (???)

Protection Circuit

- Provides interface between pads & FEC
- What details should we consider?
- How much space should be allowed?