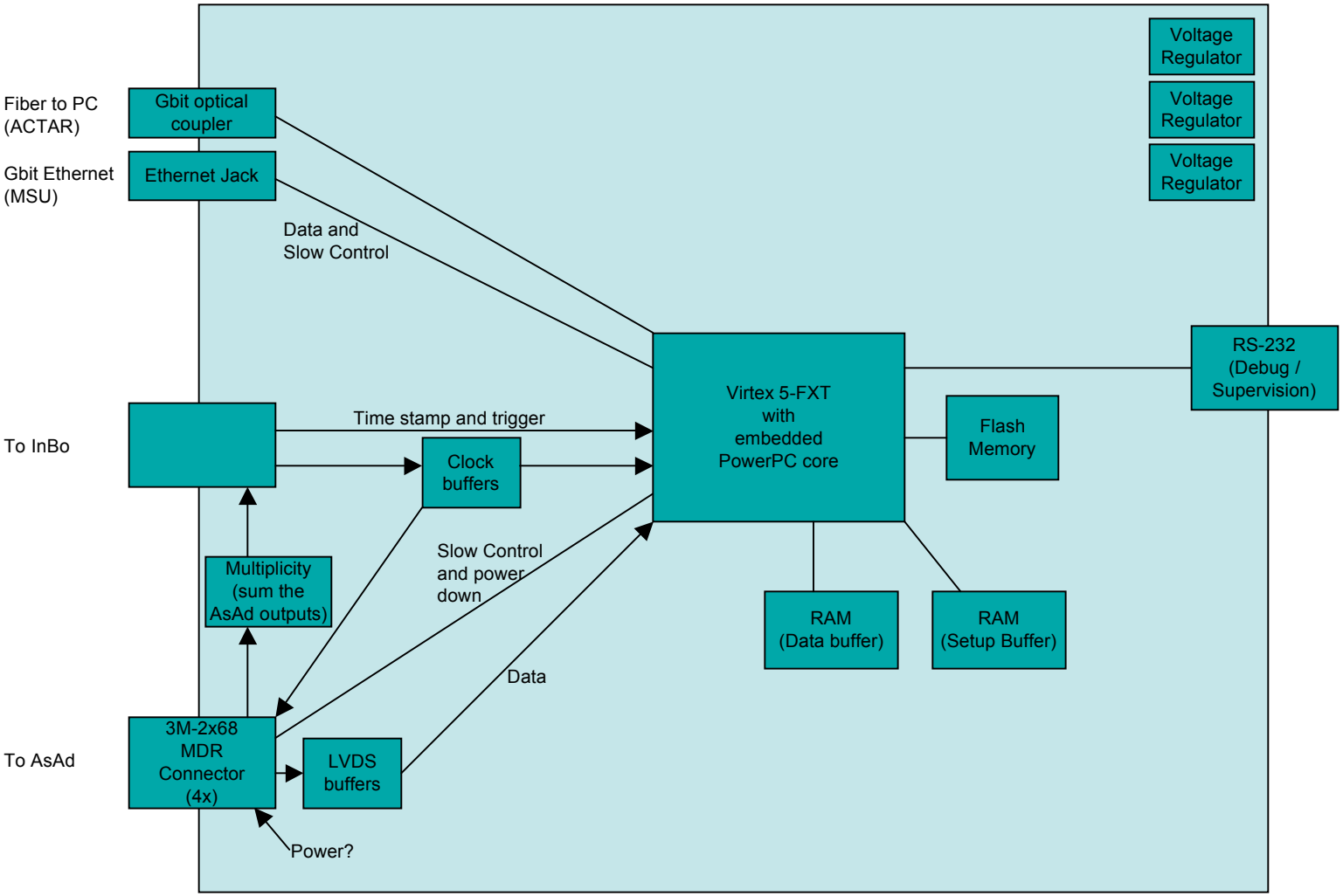
CoBo Thoughts

Michigan State University

September 25, 2008

CoBo Block Diagram



N Usher

CoBo Connectors

- To AsAd
  - ADC clock and data
    - 11 LVDS pairs
  - SCA Control
    - SCA write and read clocks (LVDS)
    - SCA write and read enables
  - Slow control to ASICs and ADC
    - 11 single-ended (SPI)
  - General Control
    - Voltage regulator power down
    - ADC power down
  - Trigger
    - To be decided be trigger group
  - Misc.
    - AsAd temperature, board id, pad id, presence detection
    - “Spy” mode
    - Power?
- To InBo
  - Master clock
  - Timestamp information
  - Trigger value from ASICs
    - To be decided by trigger group
  - Trigger signal to Cobo
- To DAQ
  - Gigabit Ethernet
    - MSU
  - Gigabit Optical Coupler
    - ACTAR
  - Use same module for both projects, with slightly different firmware

N Usher

Xilinx Starter Kit

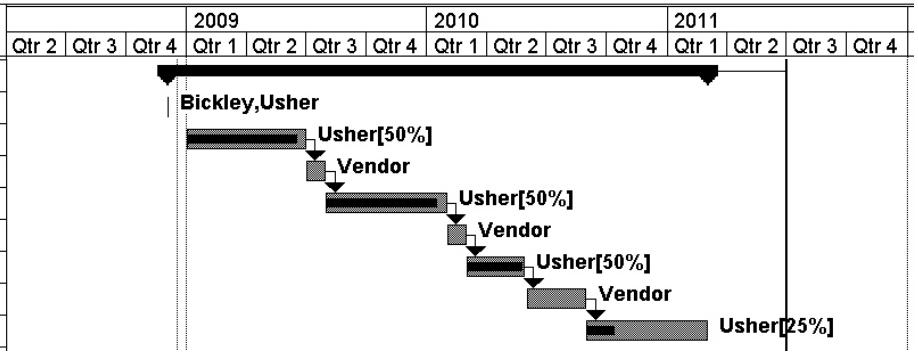
- Virtex-5 LXT Gigabit Ethernet Development Kit
  - ML505 Development Board
  - Allows test of high-speed link to AsAd ADC
  - Easy development of Gigabit Ethernet link (MSU) and fiber optic link (ACTAR)
- Virtex-5 LXT
  - No embedded PowerPC core
  - Otherwise similar in capability to Virtex-5 FXT

Functionality Discussion Items (Lolly)

1. Measure tensions & temperatures on the card; read & transmit where necessary
2. A means to test a number of functions, without AsAds being connected. Allow for a plug & play
3. Software means to image the slow control commands to verify the transmission up to CoBo.
4. Transmit a pulser (charge & time calibration) signal to the AsAd (Lemo) - connection
5. Read/Write of memory containing key information about the board (not the data storage memory).
6. Transmit a pulser trigger to the AsAd. - connection
7. Transmit the temperature readings from AsAd - connection
8. Transmit the SPY readings from AsAd to inspection points - connection
9. Sum of the multiplicity from the 4 AsAd (possibly via the FPGA) - connection
10. Receive the Stop SCA to transmit to the 4AsAd via the FPGA - connection
11. Transmit the power to the AsAd cards - connection
12. ADC ins/outs - connection
13. Grounding - connection
14. Clock, Reset etc - connection
15. The system should allow to have part or all of the AsAd AGET not functioning/switched off.
16. The system should allow having less then 4AsAd plugged in
17. FPGA functions
    - A. Configure the AGETs parameters
    - B. Read the AGETs parameters
    - C. Automatic cell normalisation routines
    - D. Calculate/establish which channels that need to be read for a given hit register (selective-read-out).
    - E. Transmit to the multiplicity unit the structure of the event from the hit register.
    - F. Per channel & Per signal
        - a) Charge normalisation (optional?)
        - b) Stamp the time of each signal
        - c) Dynamic or Static base-line calculation
        - d) Base-line subtraction
        - e) Zero removal
        - f) CFD time extraction (optional)
        - g) Pulse-height extraction (optional)
        - h) Detection of pile-up or unwanted signals (optional?)
        - i) Re-Order the channels to have a geometrical order (i,j) (optional)

Proposed Timeline

ID	Task Name	Duration	Procurement Cost	NSCL Actual Work
19	**CoBo**	**586 days**	**$32,400.00**	**1,441 hrs**
20	Test Kit & Software	1 day	$2,400.00	1 hr
21	Chip Programming & Board Layout	130 days	$0.00	480 hrs
22	Prototype I	22 days	$10,000.00	0 hrs
23	Prototype I Testing	131 days	$0.00	480 hrs
24	Prototype II	21 days	$20,000.00	0 hrs
25	Prototype II Testing	64 days	$0.00	240 hrs
26	Production	66 days	$0.00	0 hrs
27	Contigency	131 days	$0.00	240 hrs



(Note: NSCL fiscal year begins in October)

Contingent upon: 1) Lab allocation of Nathan's effort to project
2) Prompt definition of system specifications