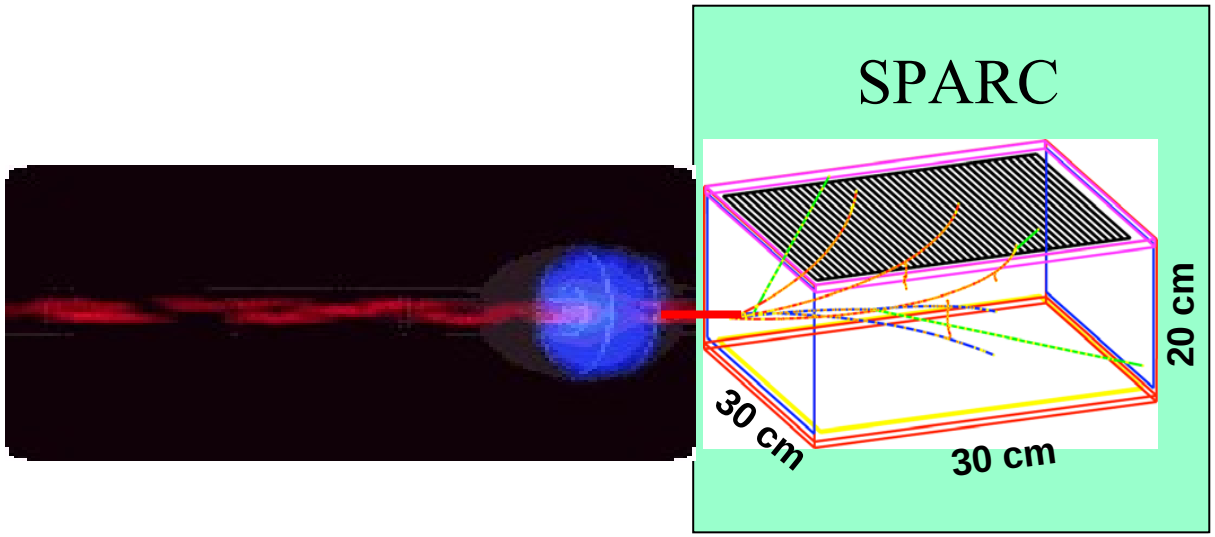
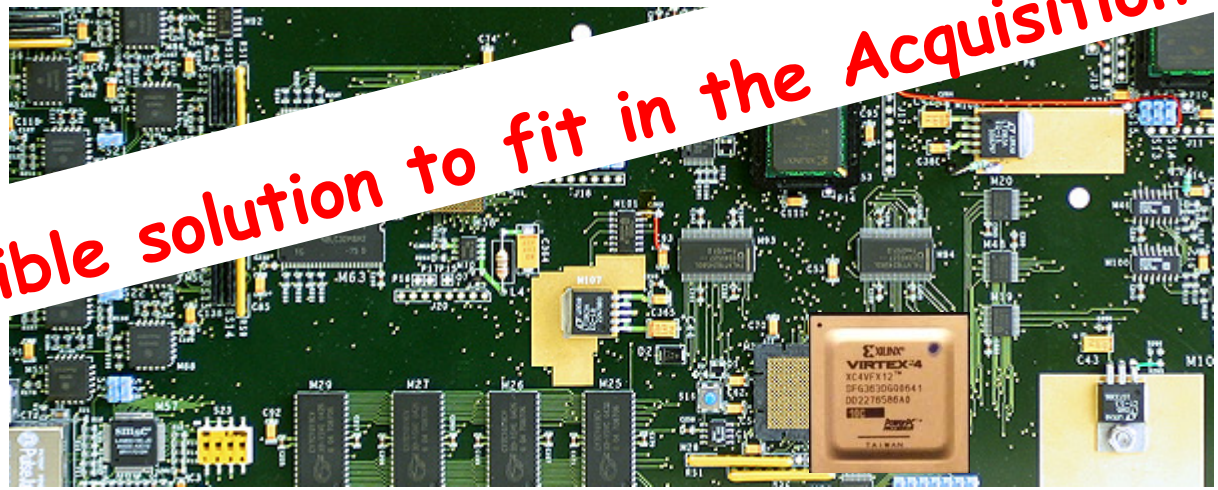


A possible solution to fit in the Acquisition hardware



About data alignment & Deserializer in Xilinx FPGA

64-tap delay element: Tidelay_resolution ≈ 74ps
So 63*74ps, up to 4.66 ns (more than half a period @ 120 or 150 MHz)

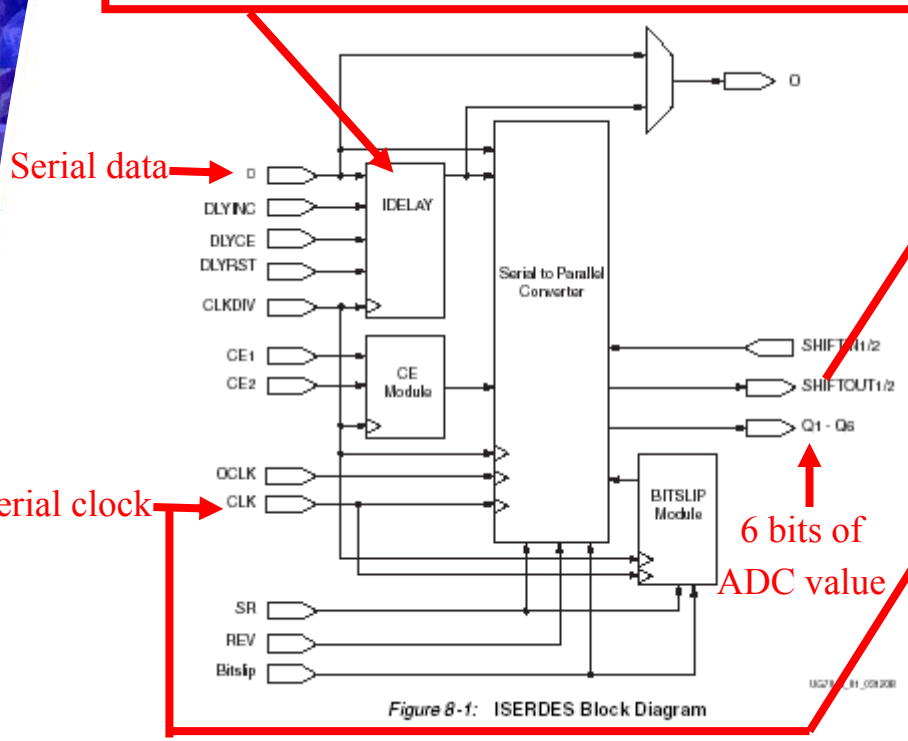


Figure 8-1: ISERDES Block Diagram

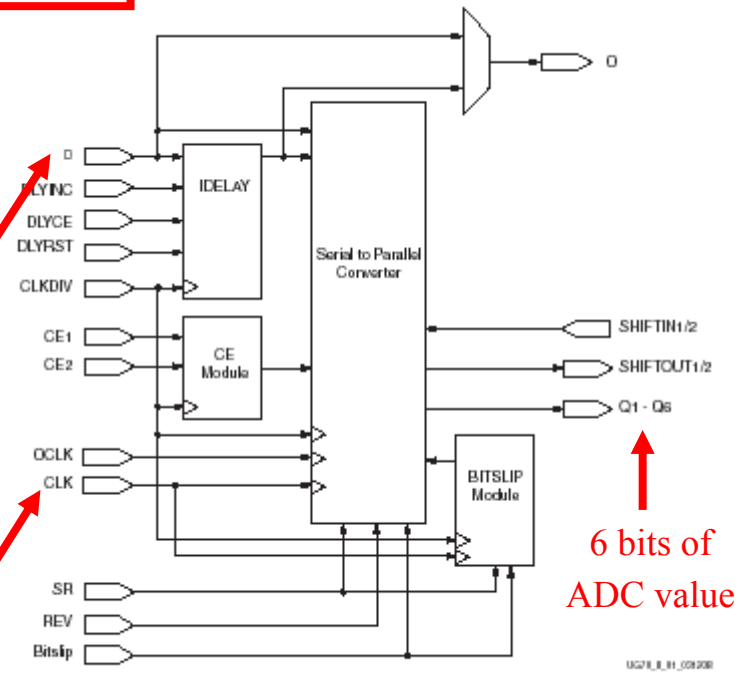


Figure 8-1: ISERDES Block Diagram

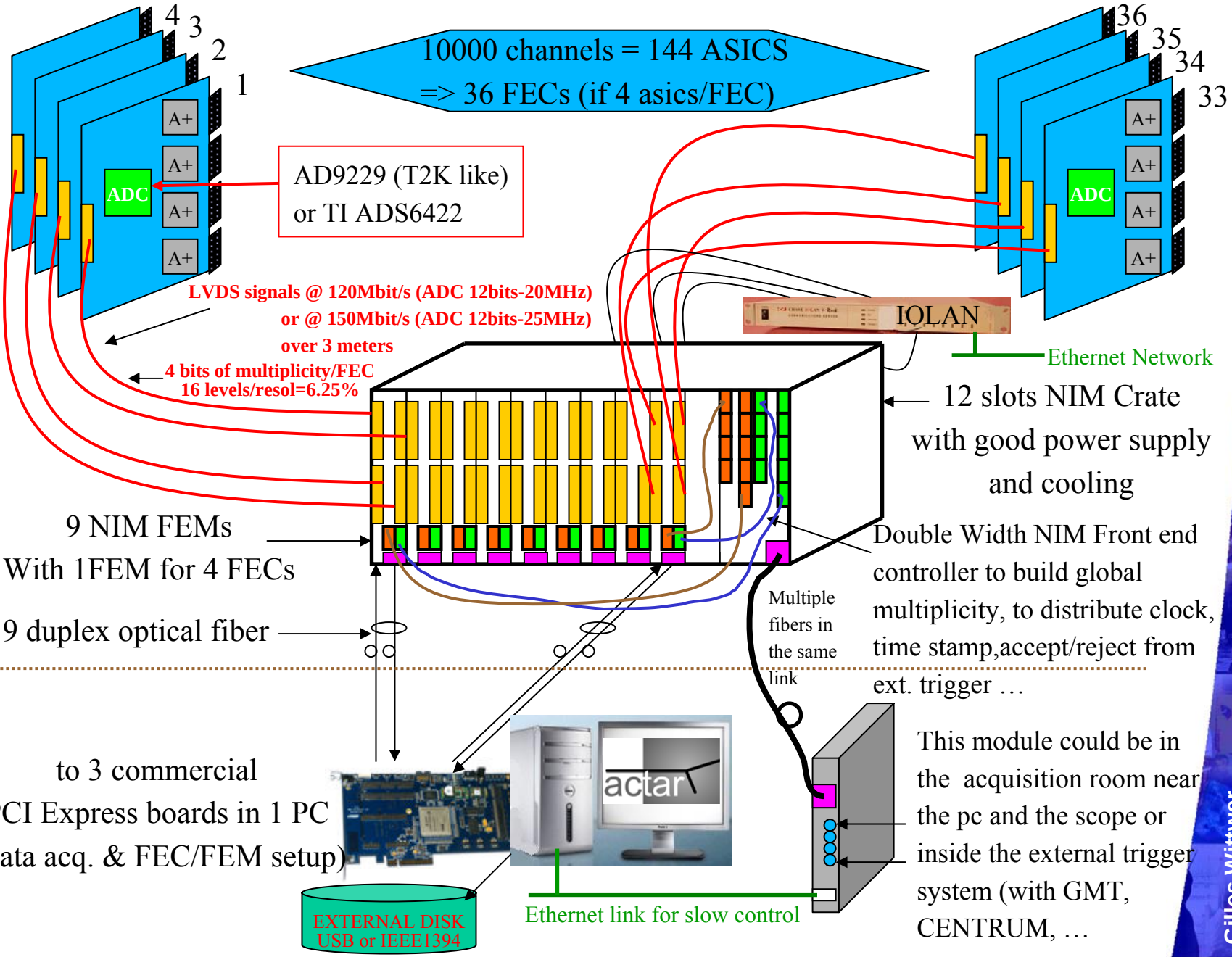
Input Serial-to-Parallel Logic Resources (ISERDES)

The Virtex-4 FPGA ISERDES is a dedicated serial-to-parallel converter with specific clocking and logic features designed to facilitate the implementation of high-speed source-synchronous applications. The ISERDES avoids the additional timing complexities encountered when designing deserializers in the FPGA logic.

2 ISERDES to convert the high speed data stream from the ADC (150 Mbit/s) to 12 bits parallel value

Xilinx Press Release and application note @ http://www.xilinx.com/prs_rls/2007/silicon_vir/0760_v4adc.htm

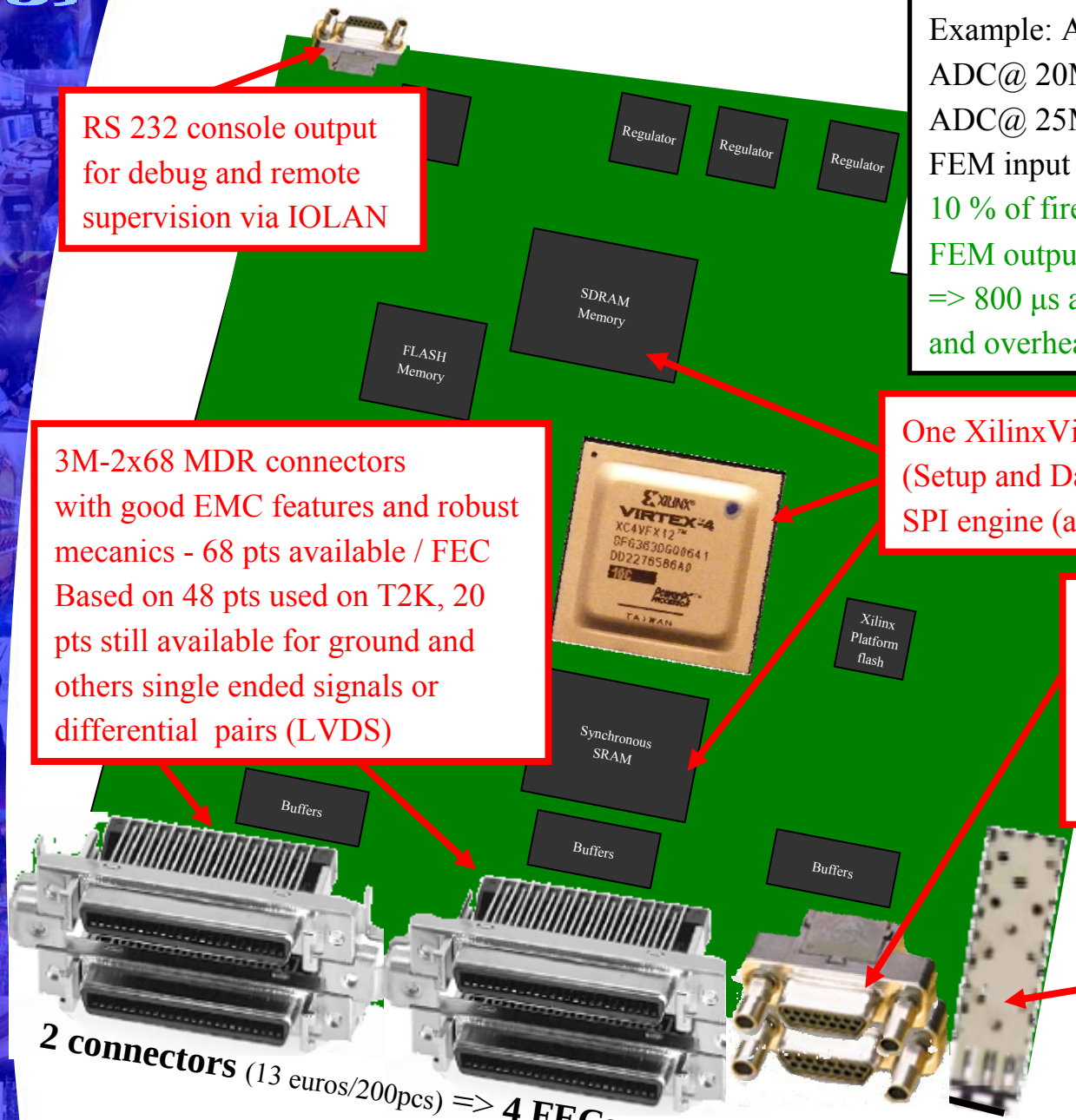
Global architecture proposal



NIM FEM board details

Example: ACTAR @GANIL
ADC@ 20MHz(T2K): 72 x 511 x 50ns ≈ 1.839 ms
ADC@ 25MHz: 72 x 511 x 40ns ≈ 1.47ms
FEM input data rate 4 x 300 Mbit/s (12bits/25 MHz)
10 % of fired channels: Tconv. = 147 µs
FEM output data rate @ 1Gbit/s: Ttransfer ≈ 50 µs
=> 800 µs available for data treatment (zeros sup.) and overhead while keeping 1KHz of counting rate.

RS 232 console output for debug and remote supervision via IOLAN



One XilinxVirtex 4 FX with enough external memory (Setup and Data buffers) with at least 1 processor for SPI engine (asics) and board supervision

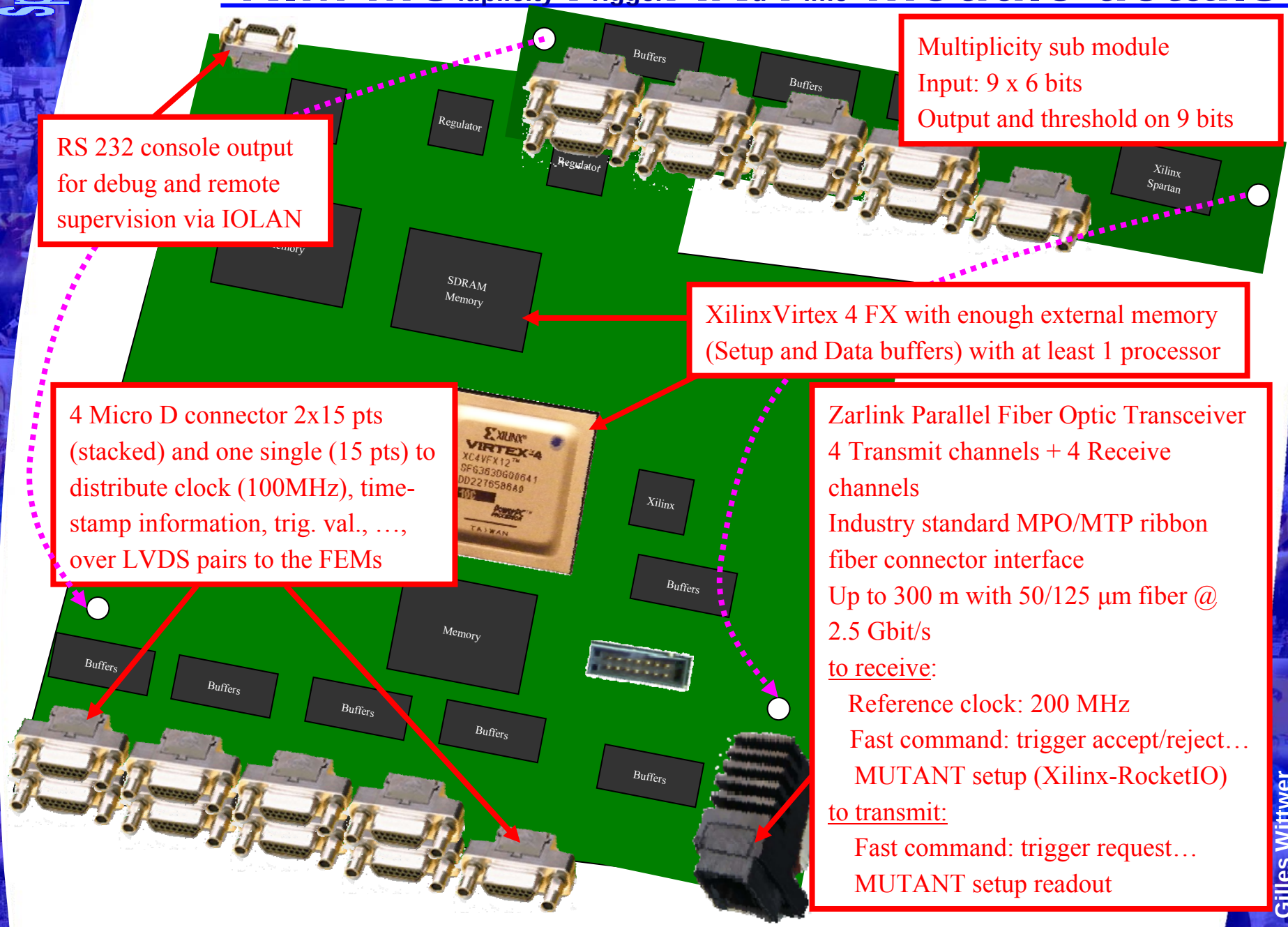
3M-2x68 MDR connectors with good EMC features and robust mecanics - 68 pts available / FEC
Based on 48 pts used on T2K, 20 pts still available for ground and others single ended signals or differential pairs (LVDS)

Stacked 15 pts Micro D connector
One to receive clock (100MHz), time-stamp information, trig. val., …
The 2nd to transmit the digital multiplicity (ex: 6 bits/4 FECs)

2 connectors (13 euros/200pcs) => **4 FECs**

One SFF (or SFP) Gbit optical coupler for duplex fiber used as acquisition channel in TX way and setup/slow control in RX way (Xilinx-RocketIO)

NIM MUltiplicity Trigger ANd Time module details



RS 232 console output for debug and remote supervision via IOLAN

Multiplicity sub module
Input: 9 x 6 bits
Output and threshold on 9 bits

XilinxVirtex 4 FX with enough external memory (Setup and Data buffers) with at least 1 processor

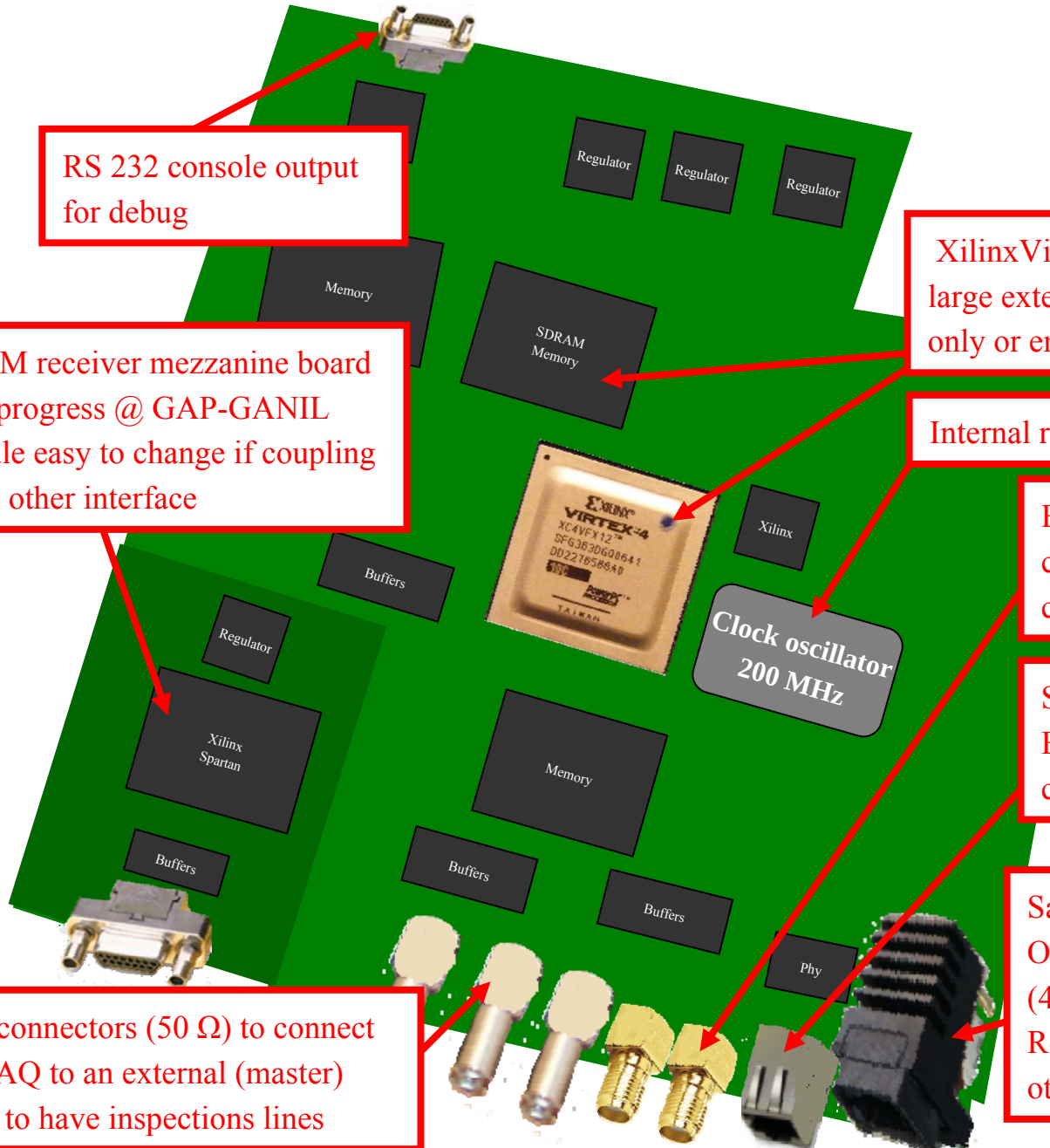
4 Micro D connector 2x15 pts (stacked) and one single (15 pts) to distribute clock (100MHz), time-stamp information, trig. val., …, over LVDS pairs to the FEMs

Zarlink Parallel Fiber Optic Transceiver
4 Transmit channels + 4 Receive channels
Industry standard MPO/MTP ribbon fiber connector interface
Up to 300 m with 50/125 µm fiber @ 2.5 Gbit/s

<u>to receive</u>:
- Reference clock: 200 MHz
- Fast command: trigger accept/reject…
- MUTANT setup (Xilinx-RocketIO)

<u>to transmit:</u>
- Fast command: trigger request…
- MUTANT setup readout

NIM BackEndModule Details



RS 232 console output for debug

XilinxVirtex 4 FX (PPC405) with large external memory (TCP/IP stack only or embedded Linux)

CENTRUM receiver mezzanine board design in progress @ GAP-GANIL
Sub module easy to change if coupling require an other interface

Internal reference clock (TCXO,VCXO)

External reference clock via SMA connectors (diff.)

Setup done through an Ethernet (RJ 45) connector

Same Parallel Fiber Optic Transceiver (4 Transmit channels + 4 Receive channels) at the other end

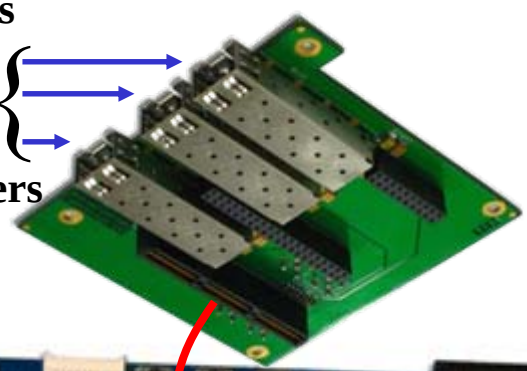
LEMO 00 connectors (50 Ω) to connect the TPC DAQ to an external (master) trigger and to have inspections lines

Xilinx V4 back end card details

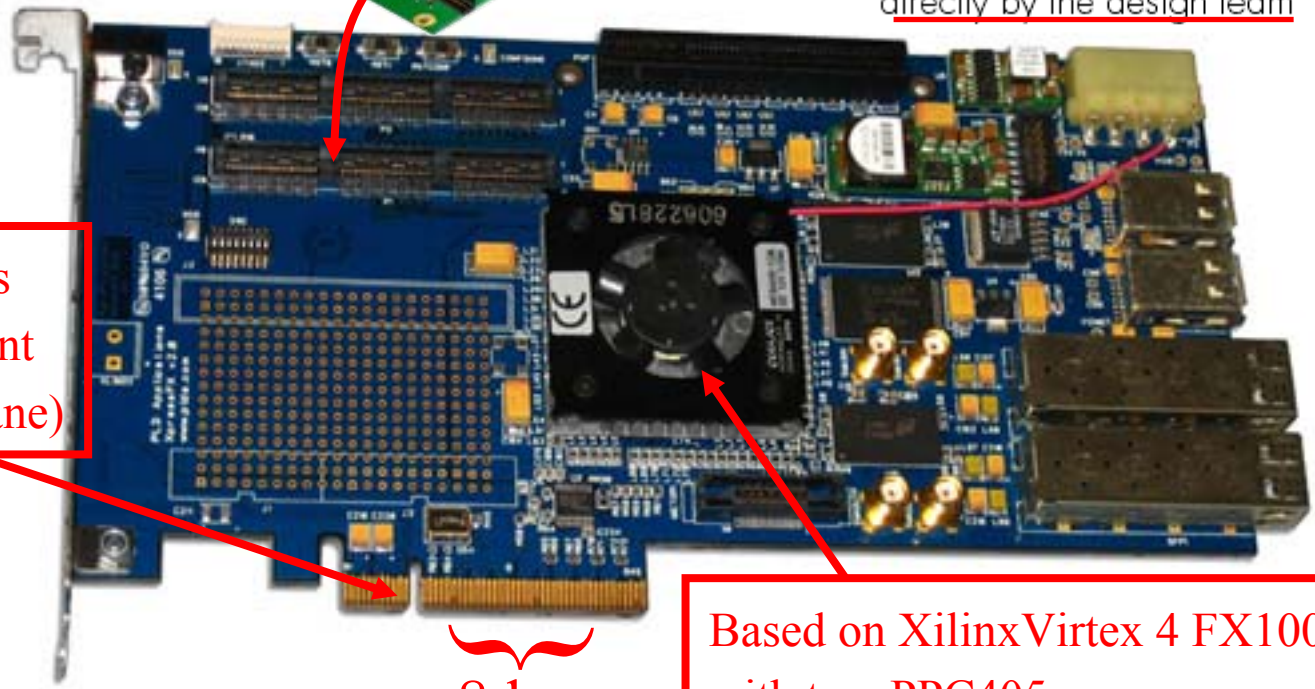
PCI Express boards from PLDA company

(provider for CERN, LOS ALAMOS lab.,…)

Up to 3 duplex fibers by PCIe board via SFP optical Gbit transceivers



- Configurable IP Core for PCIe
- PCI Express Testbench
- Reference Design
- Software Development Kit (SDK)
- Complete technical documentation
- Technical support and maintenance provided directly by the design team



PCI Express 1.0a compliant (2.5 Gb/s by lane)

x 8 lanes

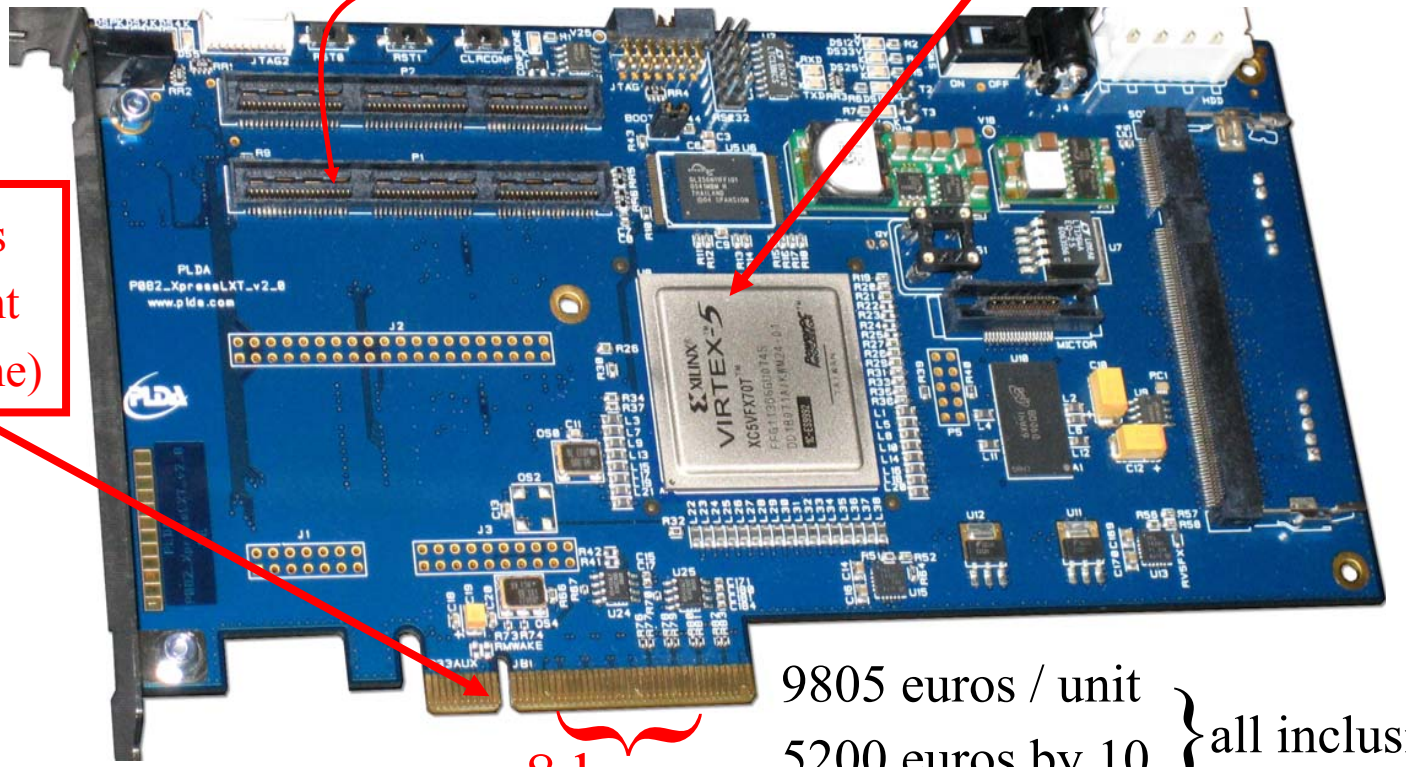
Based on XilinxVirtex 4 FX100 fpga with two PPC405 processors + 128 MB of DDR2 SDRAM

3579 euros / unit
2950 euros by 10
} all inclusive

Xilinx V5 back end card details

3 duplex fibers
by PCIe board
via SFP
optical Gbit transceivers

New XilinxVirtex 5 FX70T fpga
with two PPC440 processors
+ 128 MB of DDR2 SDRAM



PCI Express
2.0 compliant
(5 Gb/s by lane)

x 8 lanes

9805 euros / unit
5200 euros by 10
} all inclusive

Conclusion

✓ In terms of performances

- Input Counting Rate of 2 or 3 kHz seems reachable with 511 cells/ch with 10% of fired channels
- Worst case for a full readout is less than 500 Hz of ICR

✓ In terms of work (and manpower …)

- Minimum of 5 boards to design (2 years/ board with hardware and firmware)
- Two types of FEC, one FEM, one MUTANT module and one BEM

✓ In terms of budget for a serial production (except the FEC)

- 9 FEMs : 9 x 2000 euros	=	18000
- 1 MUTANT module	=	3000
- 1 BEM module	=	3000
- 1 NIM crate	=	5000
- 1 IOLAN	=	2000
- 2 PC (Setup & ACQ)	=	3000
- 3 PCI express boards (V4)	=	9000
- Duplex fibers, cables …	=	2000

TOTAL = 45000 euros ⇨ 4.5 euros/channel