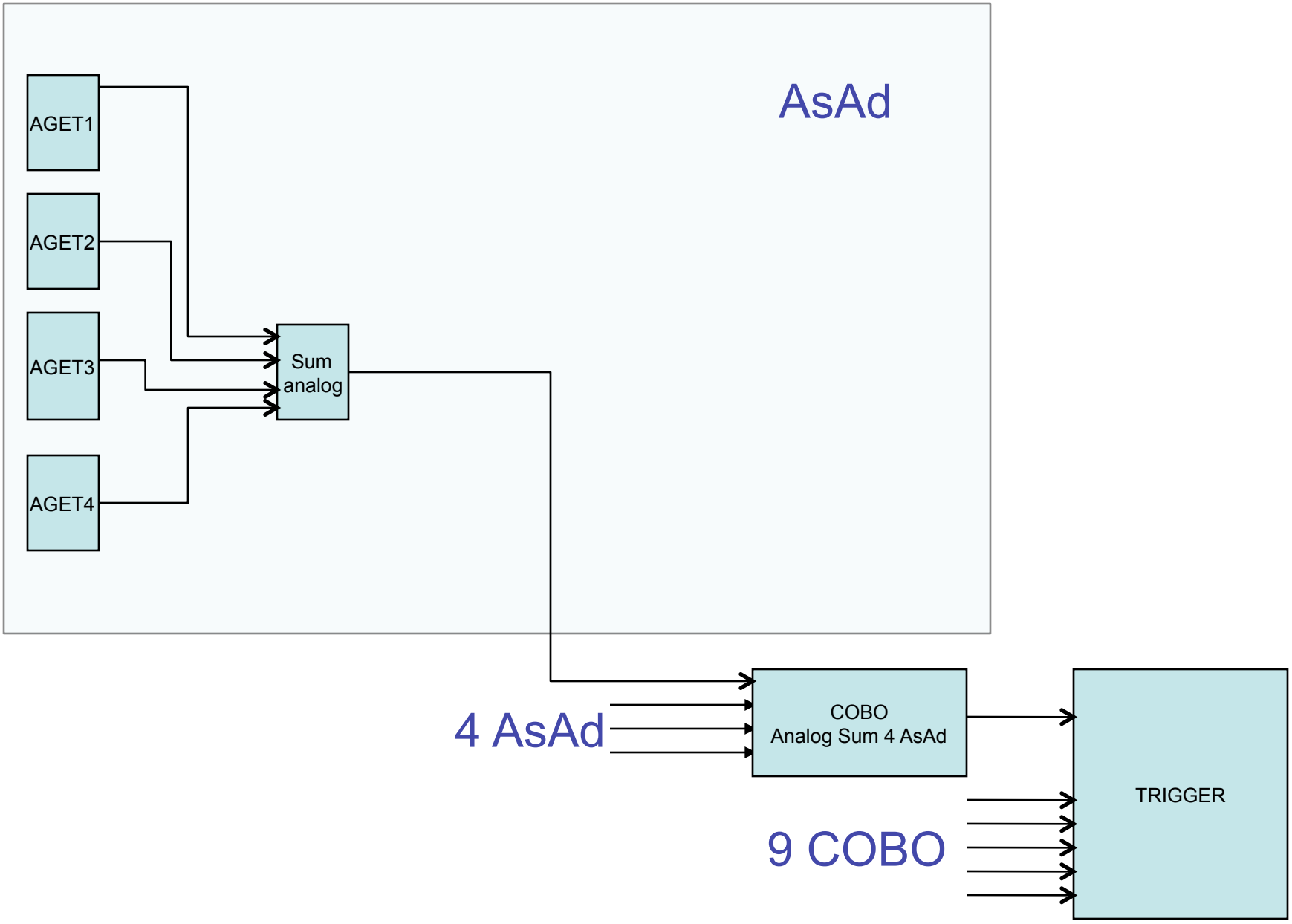
Trigger data analog up to trigger with memory of Aget multiplicity version 3; synchronized devided SCA-clock



Trigger Data Pipeline

- In the Aget, an analogical sum of logic signals is made, the time duration of minimum should be about 100ns-400ns, max 2µs (eventually longer not to have problems with ringing)
- On the AsAd board, there is an analogical sum of the 4 AGET
- On the COBO board, there is an analogical sum of the 4 ASAD, this sum signal is transmitted to the TRIGGER.
- On the Trigger board there is an FPGA, synchronized with the SCA clock, that is on this board converted by an ADC and an FPGA integrates the output of the ADC with a sliding time window