

The ALICE TPC Readout Control Unit

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Abstract- The Front End Electronics for the ALICE Time Projection Chamber (TPC) consists of about 560000 channels packed in 128-channel units (Front End Card). Every Front End Card (FEC) incorporates the circuits to amplify, shape, digitize, process and buffer the TPC pad signals. From the control and readout point of view the FECs are organized in 216 partitions, each being an independent system steered by one Readout Control Unit (RCU). The RCU, which is physically part of the on-detector electronics, implements the interface to the Data Acquisition (DAQ), the Trigger and Timing Circuit (TTC) and the Detector Control System (DCS). It broadcasts the trigger and clock information to the FECs, performs the initialization and readout via a high bandwidth bus, and implements monitoring and safety control functions via a dedicated I2C-like link. This paper addresses the architecture and the system performance of the RCU.

I. INTRODUCTION

The ALICE TPC [1, 2] is readout at both end-caps by classical multi-wire proportional chambers with cathode pad readout segmented in 557568 elements. Each pad is equipped with a readout chain [3] consisting of four basic functional units: a charge sensitive shaping-amplifier, a 10-bit 25-MSPS ADC, a pipelined digital processor and a multi-acquisition memory. The analogue functions are realized in a 16 channels custom integrated circuit (PASA). The rest of the readout chain is integrated in a single chip, named ALTRO [4], which also handles 16 channels.

When a Level-1 trigger is received, a predefined number of samples (*acquisition*) are temporarily stored in a data memory. Upon Level-2 trigger arrival the latest *acquisition* is frozen, otherwise it will be overwritten by the next acquisition. An *acquisition* contains a maximum of 1000 samples per channel. The Digital Processor implements several algorithms that are used to condition and compress the signal. It produces a certain number of non-zero data packets, thus reducing the overall data volume. Each data packet is formatted with its time stamp and size information useful for the afterwards reconstruction. The output of the Data Processor is sent to a Data Memory of 4Kx10-bit words, able to store up to 8 *acquisitions*. The data is read out from the chip

at a 40 MHz through a 40-bit wide bus, yielding a total bandwidth of 200 MByte/s.

The complete readout chain is contained in the FECs [5], which are connected to the detector by means of short capton cables. Each FEC contains 8 PASA and 8 ALTRO chips, for a total of 128 channels. A number of FECs (up to 25) are controlled by a Readout Control Unit (RCU) that contains the interface to the DAQ, the Trigger, and the Detector Control System. From the physical point of view, the two TPC readout planes are segmented in 2x18 sectors, each covering 20 degrees. Every TPC sector (15488 channels) is readout by 6 partitions (121 FECs) for a total of 216 partitions.

One of the main requirements of the RCU is set by the extremely large data volume produced by the TPC. As mentioned above, the signals produced by the TPC pads can be sampled up to 1000 times per event, thus generating about 710 MByte/event. ALICE will operate its TPC at a maximum trigger rate of 200 Hz in Pb-Pb running and 1 kHz in p-p running, producing respectively 142 GByte/s and 710 GByte/s of uncompressed data. After the data compression applied in the FECs, the data volume is reduced to 20GByte/s and 5GByte/s, respectively. Therefore, in order to be able to cope with these data throughputs, the ensemble of the RCUs has to provide a link to the DAQ with an aggregate bandwidth above 20GByte/s. This bandwidth must not decrease below 5GByte/s in the case of high rates of small data packets, like in the p-p scenario.

The radiation load on the TPC is low ($1\text{krad} \oplus 1011$ neutrons/cm² over 10 years). Thus standard radiation-soft technologies are suitable for the implementation of this electronics. However, some special care should be taken to protect the system against potential damages caused by Single Event Effects.

The RCU, originally conceived and developed for the readout and control of the ALICE TPC electronics, is being employed for the readout of other ALICE detectors (PHOS and FMD), which have a readout electronics also based on the ALTRO chip. However, the requirements in terms of bandwidth for these applications are less stringent as compared to the TPC.

II. SYSTEM ARCHITECTURE

Although primarily developed as a readout controller for the ALICE TPC FEE, the RCU has been designed to implement control, readout and monitoring functions for any front-end card based on the ALTRO chip. Therefore, while the interface to the front-end units and the core functions are tailored to the ALTRO architecture, the interface to the back-end systems (DAQ, DCS and Trigger) should be open to accommodate different technologies and possible upgrades. The resulting architecture and physical layout consist of a board containing a main FPGA, which implements all functions related to the control, configuration, readout and monitoring of the front-end units, on which the interface boards to the specific back-end systems can be plugged as mezzanine cards. In the ALICE case, these two mezzanine cards are the Detector Data Link Source Interface Unit [6] (DDL SIU), which implements a full duplex 200MByte/s optical link and is the ALICE standard interface to the DAQ, and the DCS/Trigger interface card [7], which is also an item common to a number of other ALICE detectors. In particular, the latter incorporates the LHC TTCrx chip [8], through which it receives the clock and trigger information by the TTC system, and implements an intelligent controller and DCS interface based on a FPGA with an embedded processor and an Ethernet Interface.

From the functional point of view the RCU consists of four main blocks shown in fig.1: 1) the ALTRO Bus Controller, which implements all functions related to the communication to the front-end units during the configuration and data readout, and it is described in the sections III.A, III.B and III.C; 2) the Monitoring and Safety Module, which implements the functions described in Section III.D; 3) the interface to the DDL-SIU, which implements a bi-directional synchronous 40 MHz 32-bit interface protocol to transmit the trigger related data to the DAQ and receives the configuration data for the front-end units; 4) the interface to the DCS/Trigger board implements a synchronous 40 MHz 32-bit data 16-bit address protocol to receive trigger information, configuration data for the front-end units, and transmit to the DCS different parameters relevant to monitor the behaviour of the entire front-end electronics.

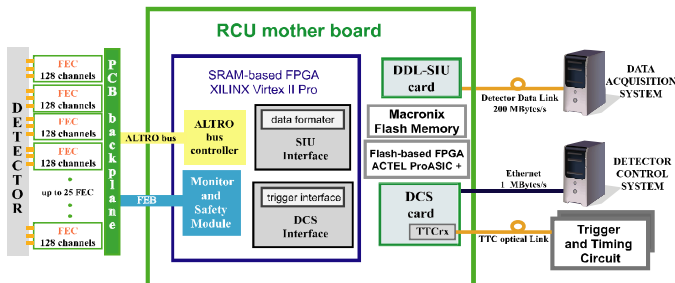


Fig. 1. The architecture of the TPC readout electronics. Up to 25 FECs are interfaced via 2 separate branches of the ALTRO readout bus and the local Slow Control link, while 2 other optical links and an Ethernet connection interface the RCU respectively to the Read Out Receiver Card, the Trigger Timing Circuit and the Detector Control System.

The second part of this section focuses on the description of the two interface buses between the RCU and the front-end unit: the ALTRO bus and the Front-end Control Bus.

A. ALTRO bus

For the initialization and data readout, the communication between the RCU and the FECs is implemented via the ALTRO bus on a PCB backplane. The ALTRO bus is essentially an extension of the FEC's internal bus that allows the RCU to access the FEC's internal components. It is a multi-drop single-master bus, whereas the RCU is the MASTER unit and the FECs are the SLAVES. In order to minimize the length of the bus lines and increase the bandwidth between FECs and RCU, the ALTRO bus Controller supports two branches running in opposite direction. Electrically the bus signals are implemented as GTL lines with the exception of the sampling clock that is transmitted to the FECs as differential PECL.

The ALTRO bus implements an asynchronous handshake [9] between the RCU and the ALTRO chips. A synchronous block transfer enhances the protocol whereas words are transferred without any acknowledgement. The bus consists of 40 bidirectional data lines for the transmission of data and addresses, and seven control lines. Special lines are used to distribute the trigger and clock signals. The ALTRO chip recognizes a set of Instructions. By means of these the RCU can access the ALTROs in the partition to write/read Configuration/Status Registers (CSR), issue Commands or read the multi-acquisition memories. The ALTRO chip acknowledges the execution of any instruction. Special cases are represented by the write broadcast instruction, where all chips in the partition are concurrently addressed, and the data readout procedure, where the ALTRO acts as a master and strobes data on the RCU data FIFO (slave) synchronously without any acknowledgement. When an instruction is issued, the Command Strobe line (CSTB) must be held low until the ALTRO asserts the Acknowledge line (ACK). ACK is kept low until CSTB is de-asserted (see fig. 2 for the Read instruction and fig. 3 for the Write Instruction and Readout). Due to this handshake, the maximum data throughput that can be reached with single write or read transactions (e.g the configuration of the ALTRO chips) is 6 MByte/s.

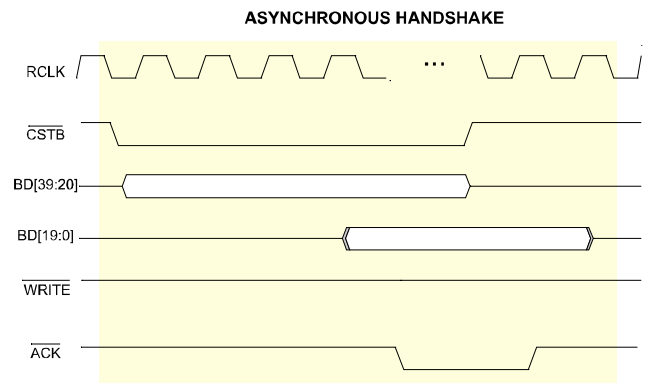


Fig. 2. ALTRO bus Read instruction chronogram.

During the Readout operation all 40 data lines are used together to transfer 40bit-long words strobed by the Data Strobe signal (DSTB) with the frequency of the system clock (40 MHz) (fig.3). The resulting bandwidth is of 200 MByte/s per branch (400 MByte/s per RCU partition).

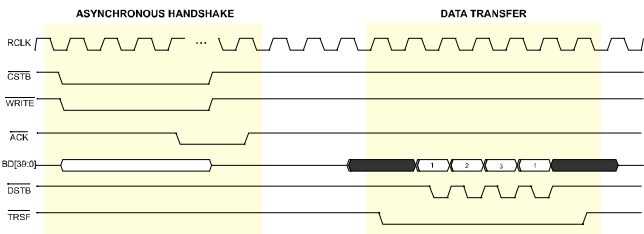


Fig. 3. Readout chronogram: after the Readout instruction (write cycle) issued by the RCU, the ALTRO asserts the Transfer line (TRSF) and makes use of all 40 bit lines to transfer data words at the clock rate.

B. Front-end Control Bus (FCB)

As we have seen in the previous paragraph, the RCU performs the configuration and readout of the FECs via the ALTRO bus. However, the FEC contains a circuit, named Board Controller (BC), implemented in a FPGA, which provides the RCU with an independent access to the FEC via a serial bus, the Front-end Control Bus. This secondary access is used to configure the FECs power state and monitor their power supplies, temperature, and the data flow. Physically, the serial bus is implemented in GTL technology as part of the ALTRO backplane.

The FCB makes use of a protocol similar to the I2C®. The main differences consist in: 1) the use of two separate unidirectional data lines instead a single bidirectional one (SDA); 2) the data bandwidth is of 2.1Mbit/s instead of the 3.4Mbit/s (I2C® Ver. 2.1 Hs-mode); 3) an additional interrupt line. The FCB begins a transaction by establishing a start condition (high to low transition of the SDA line while SCL remains high) and finishes with a stop condition (low to high transition of the SDA line while SCL remains high) (fig.4).

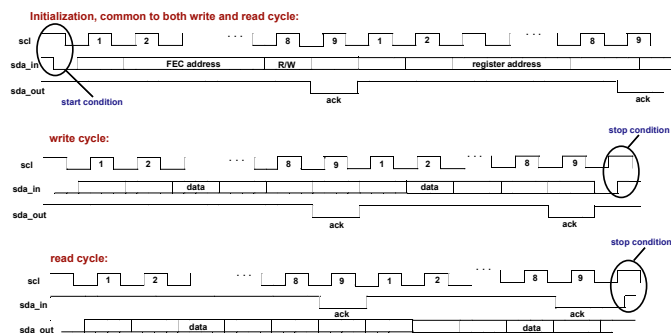


Fig. 4. Front-end Control Bus protocol. The standard I2C® SDA line is split in 2 unidirectional lines: SDA_in from the RCU to the FECs and SDA_out in the opposite direction.

Every transaction between the FCB master (RCU) and the slave (BC) requires the following sequence: start condition (1 clock cycle), eight bits containing the FEC's hardware address and the definition of the write or read cycle, eight bits with the

address of the BC internal register, 16 bits with the value of the addressed registers and a stop condition (1 clock cycle). Data bytes are synchronously transferred in nine clock cycles, eight cycles for the data bits plus one for the acknowledge information sent back from the target unit.

III. RCU FUNCTIONS

The RCU performs key system-level functions: distribution of Trigger and Clock signals to the FECs, configuration of each front-end channel, readout of trigger related data from the FECs, subsequent formatting and transfer to the DAQ system. In parallel, the RCU is also responsible for monitoring the voltages, currents, temperature and a number of functional parameters. In case any of the monitored quantities shows an anomalous behaviour, the RCU takes the appropriate action in order to prevent any damage to the FECs or severe system errors.

A. Trigger and Clock Distribution

The trigger and clock information are provided to the RCU by the LHC TTC receiver chip, TTCrx, sitting on the DCS board (figure 5). The incoming clock (RCLK) and a fixed latency Level-1 trigger pulse, originated in the A-channel of the TTCrx, are broadcasted to all FECs through the ALTRO bus. The sampling clock (SCLK) is derived from the RCLK through a PLL. Its value, which ranges from 5 to 10MHz, is distributed to the FECs via a differential line in order to minimize the noise and, therefore, the signal jitter. The Level-1 trigger word (10 bits) and Level-2 trigger messages (several bytes of information) are received from the TTCrx B-channel. The Level-1 word and part of the Level-2 message are copied in the event data packet header shipped to the DAQ. The Level-2 message is used to compare the LHC bunch crossing number with the local one, and to generate the Level-2 accept/reject signals for the FECs.

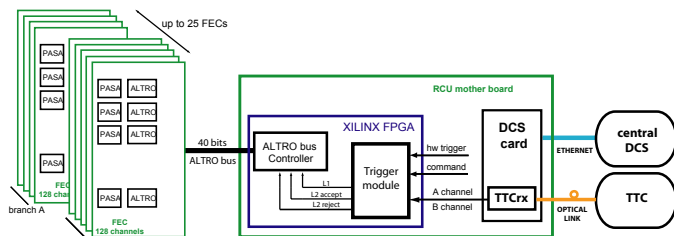


Fig. 5. FEE trigger distribution scheme

Besides the TTC chain, the RCU supports two additional trigger sources: a software test trigger, which is transmitted to the RCU as command, via the DDL or the DCS, and a hardware test trigger, via a dedicated input connector.

B. Configuration of the front-end units

The configuration parameters for the ALTROs and BCs are stored in the RCU Instruction Memory through one of the following two interfaces: the DCS or the DDL. A sequencer fetches these instructions, decodes their content and executes them in the form of a single ALTRO instruction (RCU micro instruction) or sequence of them (RCU macro-instruction). The macro instructions allow, for example, to write into the

ALTRO pedestal memory, or to verify its content. Another example is an RCU macro that handles a complete trigger sequence to exercise the readout chain.

C. Data Readout

The readout of one event is performed in two separate phases, which are consecutive for a given event, but can otherwise be activated concurrently. In a first phase the trigger information is received by the RCU and broadcasted to all modules in the subsystem, starting the digitisation of each channel, which lasts for 88 ns (TPC drift time). During this phase data processing takes place in the ALTROs. In the second phase, information is moved by the RCU from the ALTRO's multi-event buffer to the DAQ, on a channel-by-channel basis. The time needed to complete the second phase depends on the size of the event, but other triggers can be processed during the readout of the previous event, as long as the multi-event buffers in the FEC are not full. Dead time can be generated only when this condition occurs. FECs containing valid data are enabled to assert data on the bus by individual addressing, according to an Active Channel List stored in the RCU. In order to minimize the event readout time, the RCU supports a Sparse Readout mode. In this mode of operation the empty channels are flagged by the FEC BCs, avoiding their addressing by the RCU.

The readout is performed concurrently on the two ALTRO bus branches. The incoming event data is stored in two memories, working in interleaved mode, each being able to store the event data of one single ALTRO channel. While data from one memory is being pushed into the DDL, data from the next ALTRO channel is stored into the other one. The 40-bit wide ALTRO data packets are formatted into 32-bit wide packets and wrapped in the ALICE DDL data format, with 8 headers and one trailer word. A further option sets the channel readout order following the detector topology, in order to facilitate the on-line data processing. The readout chain is depicted in fig. 6.

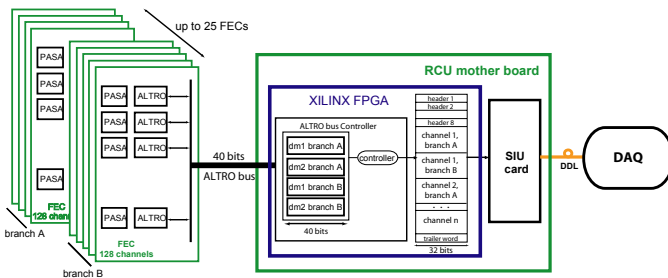


Fig. 6. FEE readout scheme.

D. Safety and monitoring

The RCU controls the power state, voltages, currents and temperature of the FECs. In detail, every FEC contains a 10-bit, 5-channel ADC with an on-chip temperature sensor and an I2C® interface. One channel provides the temperature of an embedded sensor, while the other four provide the values of the analogue and digital voltages and currents measured at the input of the FEC. The BC logic includes an I2C® master to

read this ADC. The communication between the two units is synchronized by a clock signal with a frequency of 150 kHz. At this rate, every 2ms the BC reads the 5 parameters and updates the corresponding registers. In addition, the BC contains the configuration, status and error registers, and a set of counters that measure a number of important signals (e.g. the Level-1 and Level-2). The table is accessible both via the ALTRO bus (during the configuration phase) and the FCB (in the configuration phase and data readout phase).

At power-up, the RCU downloads into the BC the reference range for the monitored quantities. As soon as one of these parameters goes out of range, the BC asserts the interrupt. The RCU starts polling the error register of each FEC to identify the error source. In the event of a hard error (temperature or currents over their thresholds, voltage under threshold, card power regulators error), the RCU switches immediately off the corresponding FEC. Immediately after, a recovery procedure will be executed to diagnose the occurred error and report to the DCS system. It is important to note that, during these operations, the communication to the other cards of the branch is not perturbed.

E. SRAM FPGA scrubbing

The use of SRAM-based FPGA required special attention to Single Event Upset. To monitor the functionality of the chip, the configuration memory of the main FPGA (VirtexII-pro from Xilinx) is continuously readout by an on-board flash-based microcontroller and compared with a mask stored in a local flash memory. Whenever an error is detected, the microcontroller is able either to reload the complete firmware of the FPGA or reconfigure just the local logic affected by SEU (scrubbing technique). Newer version of the firmware can be uploaded by the use of the DCS link.

IV. RCU PHYSICAL DESCRIPTION

The RCU is a 22.5 x 15 cm² – 8 layers PCB - board. The top side of the board is equipped with the connectors for the JTAG chain of the FPGAs, the connectors for the two mezzanine cards (SIU and DCS board) and the main power supply connector. In addition there are a 40MHz SMD oscillator (auxiliary board clock generator) and the power regulators. On the RCU bottom side (figure 7) four connectors are dedicated to the interface to the readout backplane. The GTL transceivers are located close to the connectors themselves, while other active LVDS/LVPECL transceivers take care of the distribution of the timing signals. This side contains as well the VirtexII-pro main FPGA, the Macronix Flash memory and the FPGA re-configuration microcontroller (Actel Pro-Asic+).

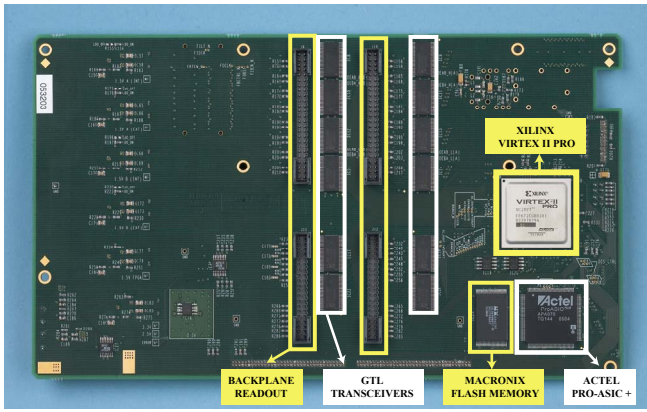


Fig. 7. RCU Mother board. On the board back side the connectors for the mezzanine cards.

V. SYSTEM PERFORMANCE

The largest readout partition consists of 3200 ALTRO channels (25 FECs). A typical configuration for such a partition consists of about 350 kbytes, and can be as large as 7 MBytes worst case (1000 10-bit pedestal values per channel). As described above, configuration data can be transferred to the RCU both via the DDL and the DCS. In both cases the data transfer takes less than 50ms for the typical configuration. The subsequent transfer to the FECs requires about 150ms. As far as the readout performance is concerned, the ALTRO bus has a measured bandwidth of 260 MByte/s and 55MByte/s for respectively the Pb-Pb and p-p running conditions. In the former case the average data block size is 200 Byte/channel and 20 Byte / channel in the latter.

The Local Slow Control network runs at a clock frequency of 5 MHz. However, its protocol requires the transmission of a large number of control words. A single 16-data bit transaction, e.g., requires 8 μ s. When an interrupt occurs, the RCU starts polling the error/status register of all FECs of one branch. This action could require up to 100 μ s in the case of a readout partition with 13 FECs/branch.

VI. CONCLUSIONS

The RCU, which is a key unit of the ALICE TPC FEE, is a board based on a main FPGA, which implements the control, readout and monitoring of the ALICE front-end cards based on the ALTRO chip. In the ALICE application it is equipped with two mezzanine cards, which implement the interface to the DAQ, and to the Trigger and DCS systems. The RCU fulfils the ALICE requirements providing an aggregate bandwidth between FECs and DDLs in excess of 34 GByte/s for the Pb-Pb running conditions, and of about 12 GByte/s in the p-p scenario.

The latest prototype has been successfully tested with a sizeable fraction of the final system. A production of about 270 RCUs has been recently completed. The installation on the detector is scheduled to start in spring 2006.

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