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saclay

AGET, a Front End ASIC for Active Time Projection Chamber

Requirements overview

Revision 2.0, January 20, 2009

List of diffusion

The following list presents the different groups involved in the definition of the requirements.
This document is managed by the CEA/DSM/IRFU/SEDI/LDEF which has in charge the design of the AGET ASIC.

ACTAR Collaboration
CENBG
MSU
R3B

Revision history

Date	Revision	Changes
28-Mar-08	1.0	Initial release
19-Jan-09	2.0	Name of the asic: AFTER+ to AGET
		Trigger and multiplicity part: architecture, width and veto time.
		Hit-channel Register: duration of the data
		ADC change: ADS6422

Contents

1. Introduction

This document defines all the requirements for the AGET chip. This paper is based on the first requirement (« white book ») and discussion occurring during the meeting in GANIL (November 2007) and Santiago de Compostela (March 2008). The trigger part has been finalized and fixed after several meeting in the end of the 2008 year.

2. General view of the architecture

The AGET ASIC is a new version of the AFTER ASIC designed for the readout of the large TPC's used in the T2K neutrino experiment. This chapter describes briefly the architecture of the AFTER chip and the main new functionalities of the further chip.

2.1 Architecture of the AFTER chip

The AFTER asic (fig. 1) has 72 channels handling each one detector pad. A channel integrates mainly: a charge sensitive preamplifier, an analogue filter (shaper) and a 511-sample analog memory. This memory is based on a **S**witched **C**apacitor **A**rray structure (**SCA**), used as a circular buffer in which the analog signal coming out from the shaper is continuously sampled and stored. In the read out phase, the 511 samples of each channel are read back, starting by the oldest sample. The analogue data from all the channels are time domain multiplexed toward a single output to be sent to an external 12-bit ADC.

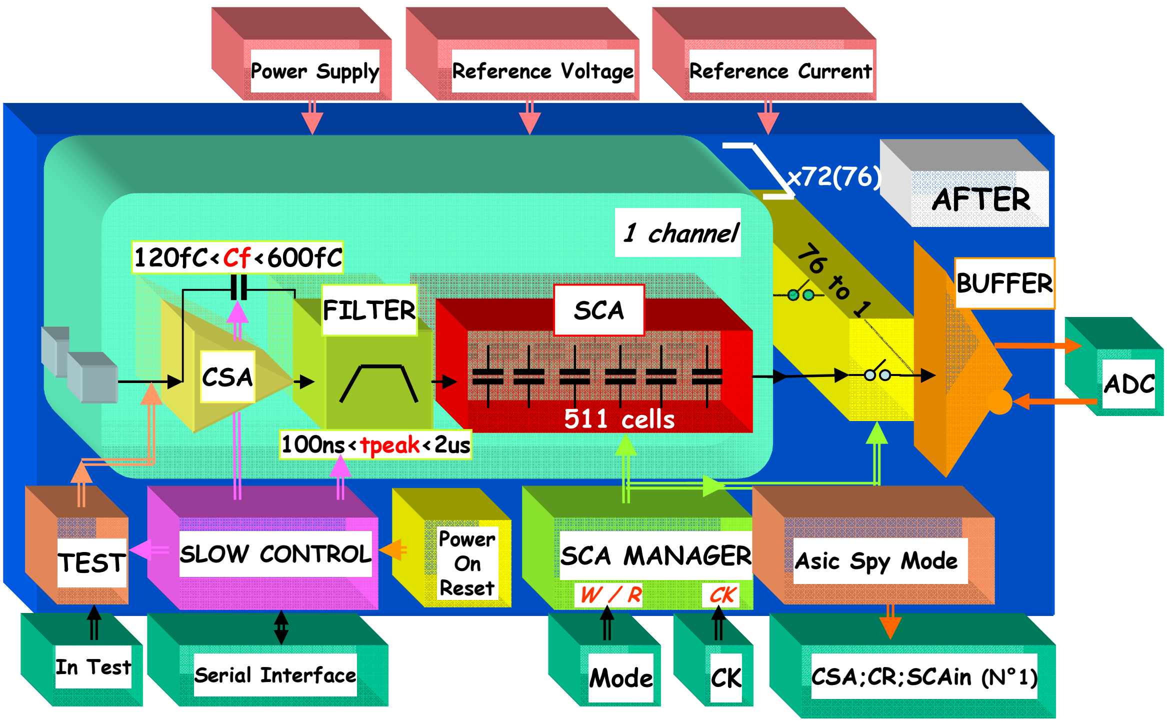


Fig 1: Block diagram of the AFTER chip.

The chip main parameters (gain, peaking time, test mode and asic control) are settable by Slow Control. Two chip inputs permit to calibrate or to test the 72 channels. A “spy” mode is available to control some internal test points (CSA & PZC outputs and SCA input) of the first analogue channel.

2.2 Architecture of the AGET chip

The architecture of AGET asic (fig. 2) is based on the one described previously with new additional features and some modifications.

These new features are:

- Possibility to bypass the internal CSA and to enter directly to the shaper or SCA inputs,
- Auto triggering: discriminator, threshold (DAC) and discriminator inhibition per channel,
- Multiplicity data: analog “OR” of the 72 discriminator outputs,
- Address of the hit channel(s),
- Several mode of channel read out: hit channel(s), several channels or all channels,
- Several mode of SCA read out: 511, 256 or 128 analog cells.
- “Spy” mode: Additional output (discriminator input??) [must be confirmed].

The modifications concern:

- The charge dynamic range,
- The peaking time range.

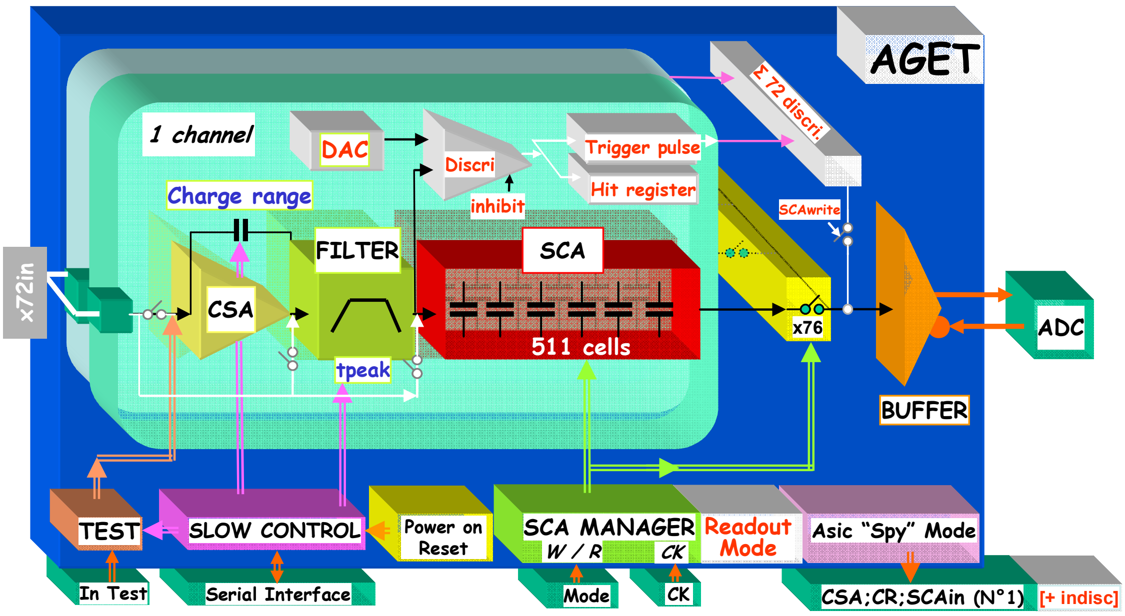


Fig 2: Block diagram of the AGET chip.

All these elements are described and analyzed more precisely in the next chapter of this document.

3. List of the requirements

3.1 Number of channel

72. This number was fixed by the granularity of the T2K module (6 x 4 x 72 pads). It was also the maximal number compatible with an acceptable silicon area.

3.2 detector signal polarity

This ASIC can operate with the both signal polarities (positive or negative) according to the adjustment of d.c voltages defined on the frond end card or inside of asic .

3.3 External Preamplifier

It is possible to bypass the internal CSA and to enter directly to the filter or SCA inputs. This feature is useful when the input dynamic range of the detector exceeds those of the ASIC or if power consumption or area constraints don't allow to put the asic on the detector.

3.4 Charge measurement

3.4.1 Input charge range

The chip must operate with three values of input dynamic range: 120 fC [750 keV], 1 pC [6.25 MeV] and 10 pC [62.5 MeV]. The full charge range must be adjusted per channel, by selecting one of the three CSA feedback capacitors (Slow Control).

3.4.2 Output voltage range

The chip must fit the input voltage dynamic of the external 12-bit ADC. The ADC chose is the ADS6422 from Texas Instruments.
The Integral Non Linearity must be less than 2 %.

3.4.3 Peaking Time

The value of the peaking time is adjustable, by sixteen discrete values, between 50 ns and 1us. This value will be common for all channels.

3.4.4 Charge Resolution

The resolution of the charge measurement must be better than $1/2^{10}$. As the resolution depends on different parameter values, we consider that the noise will be less than 850 e- r.m.s for the following configuration: charge range: 120 fC, Peaking Time: 200 ns, channel input capacitor: 30 pF.

3.5 The SCA

3.5.1 SCA memory cells

The number of analog memory cells is fixed to 511.

3.5.2 Sampling Frequency

The sampling frequency can be set from 1 MHz to 100 MHz to match with the various drift velocity of the chambers.

3.5.3 Time resolution

The sampling frequency and the stop of the sampling phase are managed outside the asic [for T2K, by the F.E.M card]. In the asic level, the sampling precision in the SCA is the convolution of two uncorrelated effects: the jitter and the skew.

3.5.3.A The jitter

Measurements have been made on the AFTER chip to extract the spread of the sampling time for a fixed cell index. The value of this effect, call sampling jitter, is **58 ps**. This value includes the jitter contributions of the clock distribution and the sampling inside the chip.

3.5.3.B The skew

Measurements have been made on the AFTER chip to extract the skew corresponding to the dependency of the sampling time with the cell index. These results (fig. 3) show that there is a difference of behavior between 2 groups of channels. For the right group (channel 37 to 72), the sampling clock and the analog signal are propagating in opposite way, minimizing therefore the value of the skew (150 ps rms). For the left group (channel 1 to 36), the sampling clock and the analog signal are propagating in same way, giving therefore a higher value of the skew (700 ps rms). The characteristics are very reproducible from chip to chip and could be even corrected off line.

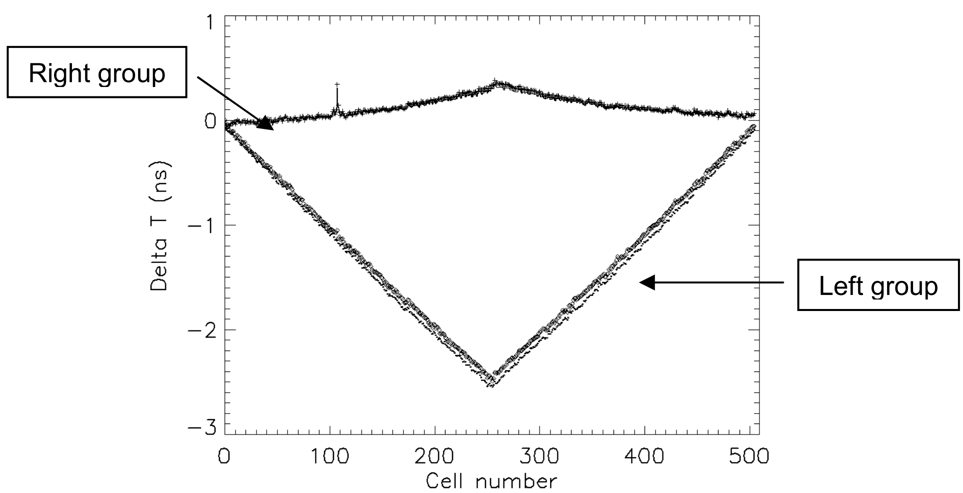


Fig 3: Variation of the effective sampling time with the cell index in the SCA.

3.6 The threshold channel

3.6.1 The discriminator solution

It is a Leading Edge Discriminator.

3.6.2 Filtering

The filtering is the one of the charge channel (fig. 4).

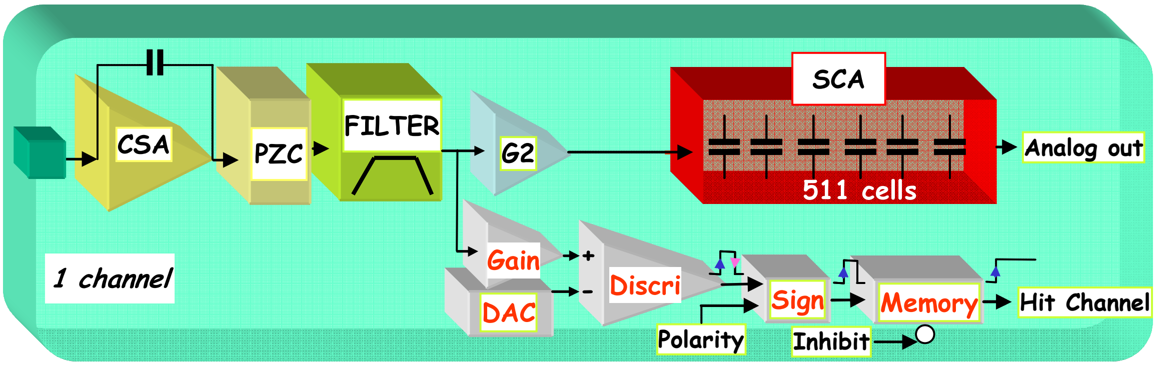


Fig 4: Block diagram of the channel.

3.6.3 Inhibition

By Slow Control, the output of the channel discriminator could be inhibited.

3.6.4 Hit channel register

The hit-channel register is set to "1" by the output signal of the discriminator and reset to "0" the second time the SCA write address pointer crosses the cell "0". This gives a length of memory time between 1 and 2 SCA write cycles (fig. 5).
This hit channel register could be read after the SCA writing phase by using the slow control link (with a specific protocol), and it will be clear during the SCA readout phase.
If a second event arrives, the time of memory will be increase by one complete SCA writing phase.

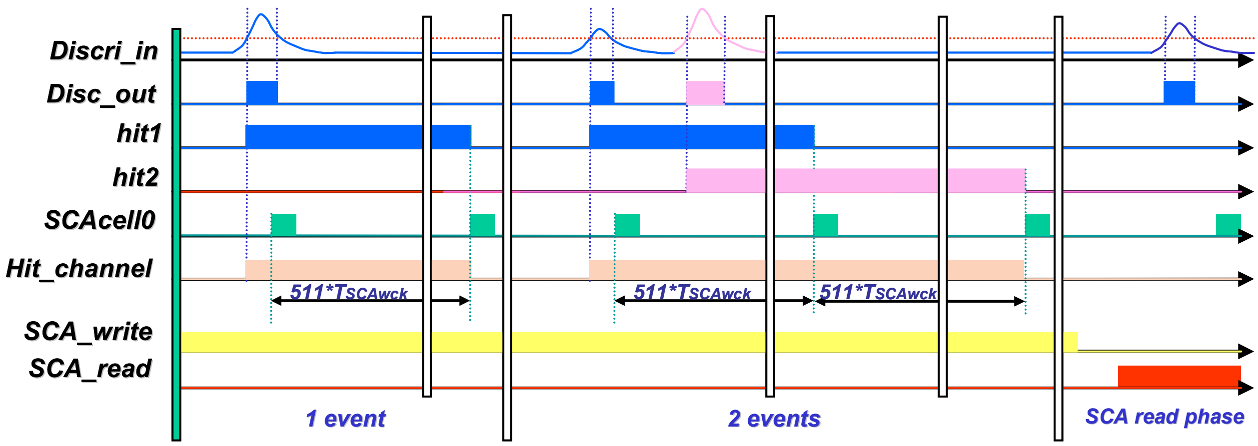


Fig 5: Hit-channel register setting.

3.6.5 Trigger output

The output signal of the discriminator gives a trigger signal (fig. 6) with a fixed value equal to twice of the SCA clock readout period (80 ns for 25MHz SCA readout clock frequency). This signal with the 71 other trigger outputs form (analogical sum) the multiplicity signal which through the unique internal analog data buffer is continuously digitized by the external 12-bit ADC dedicated also for the SCA analog data. The precision of the multiplicity measurement must be around 5 to 10%

An inhibit function must be implemented to avoid multiple triggering at the channel level during a time window. There are 3 possibilities (by slow control):
1/ any inhibit,
2/ a fixed dead-time value of 4 µs,
3/ inhibit by the hit-channel register.

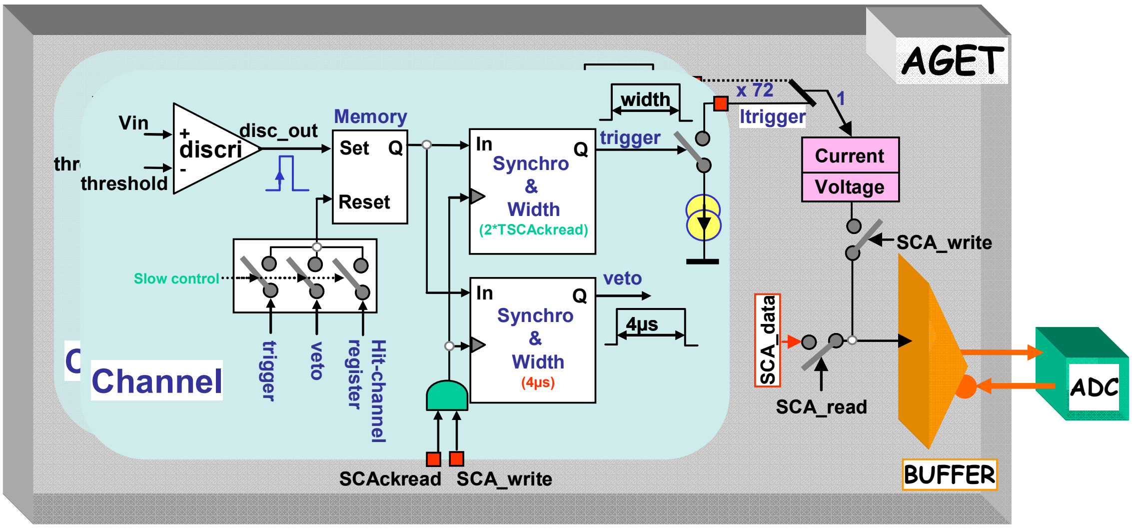


Fig 6: Principle of the trigger output.

3.6.6 Input dynamic range

The input linearity range must be equal to 5% of the channel input dynamic range. The Integral Non Linearity must be less than 5%.

3.6.7 Threshold voltage

The threshold voltage is set by 2 internal programmable DACs. The first is common of all 72 channels and has 3 bits plus 1 bit of polarity. The second DAC is attached to the channel and has 4 bits.

3.6.8 Minimum Threshold voltage

The minimum threshold voltage must be set to a value slightly higher than the noise level.

3.7 The Readout Phase

3.7.1 Readout Frequency

The readout frequency range is 20 MHz to 25 MHz.

3.7.2 The channel readout mode

There are three different modes for the read out of the channel SCAs: all the channels; only the hit channels; only specific channels.
For the two last readout modes, the address of the hit channels or of the specific channels will be given by using the serial link of the Slow Control [write and read phase].

3.7.3 The SCA readout mode

In conjunction with the previous channel readout mode, it will be possible to read the SCA according to a predefined number of analog cells: 511, 256 or 128.
The principle of operation is the following:

- **511**

It is the nominal mode. The number of readout cells is equal to the depth of the SCA (fig. 7). The maximum TPC drift time is cover by all the SCA.

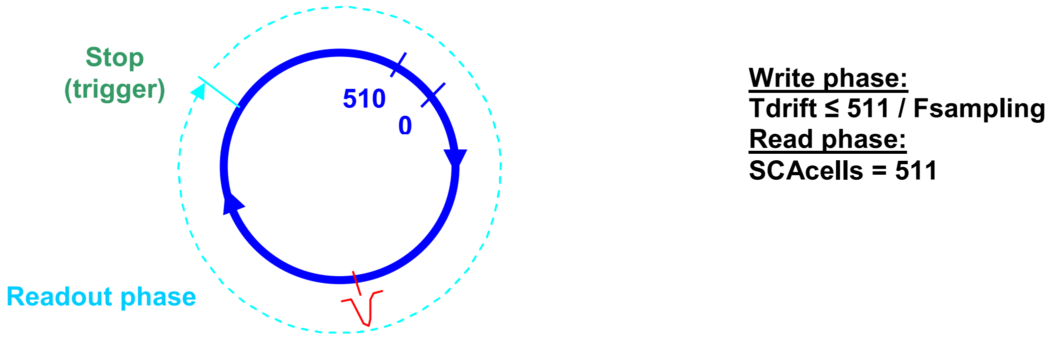


Fig 7: 511 cells readout mode.

- **256**

The number of readout cells is equal to the half of SCA depth (fig. 8). The SCA must cover two times the maximum TPC drift time. The read address of the first SCA cell is obtained by subtracting (internal logical operation) the address of the last written cell by 256.

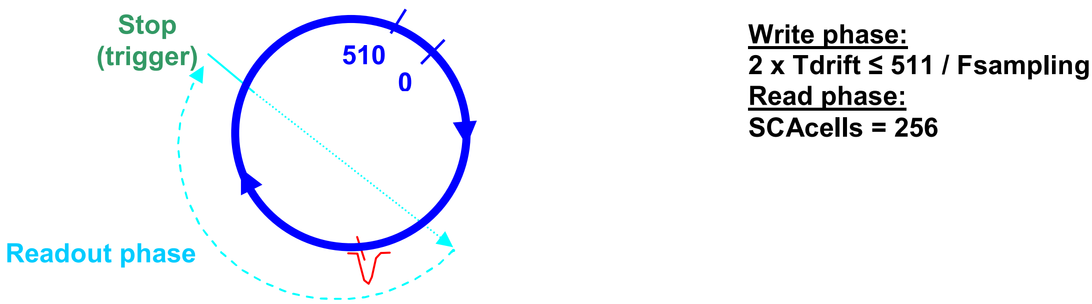
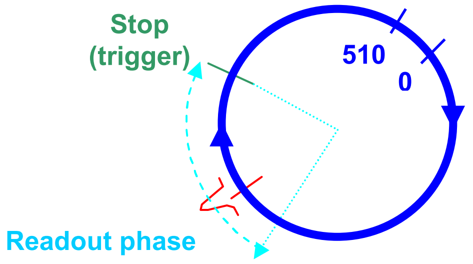


Fig 8: 256 cells readout mode.

- **128**

The number of readout cells is equal to the quarter of SCA depth (fig. 9). The SCA must cover four times the maximum TPC drift time. The read address of the first SCA cell is obtained by subtracting (internal logical operation) the address of the last written cell by 128.



Write phase:
4 x Tdrift ≤ 511 / Fsampling
Read phase:
SCAcells = 128

Fig 9: 128 cells readout mode.

3.8 The Test

The chip includes a test system useful for: electrical calibration, asic test bench and functionality control on all electronic channels [ASIC input to acquisition board].

3.8.1 Electrical calibration

An external current signal can be send to a selected channel (one among 72).

3.8.2 Test mode

In this mode, an external voltage signal is applied on one of the three internal injection capacitors (one capacitor per input charge range). The resulting current signal is send to the selected channel (one among 72).

3.8.3 Functionality mode

In this mode, an external voltage signal is applied on the test capacitor of the selected channel (1 channel, several channels or all channels).

3.9 Counting Rate

The chip must operate with a maximum counting rate of 1 kHz.

3.10 Power Consumption

The power consumption of the chip must be less than 10 mW per channel (Vdd = 3.3V).

4. Synthesis of the AGET requirements

Parameter	Value
Polarity of detector signal	Negative or Positive
Number of channels	72
External Preamplifier	Yes; access to the filter or SCA inputs
Charge measurement	
Input dynamic range	120 fC; 1 pC; 10 pC
Gain	Adjustable/(channel)
Output dynamic range	2V p-p
I.N.L	< 2%
Resolution	< 850 e- (Charge range: 120fC; Peaking Time: 200ns; Cinchannel. < 30pF)
Sampling	
Peaking time value	50 ns to 1 µs (16 values)
Number of SCA Time bins	511
Sampling Frequency	1 MHz to 100 MHz
Time resolution	
Jitter	60 ps rms
Skew	< 700 ps rms
Trigger	
Discriminator solution	L.E.D
Trigger Output/Multiplicity	OR of the 72 discriminator outputs; Width=2*TSCAckread
Dynamic range	5% of input charge range
I.N.L	< 5%
Threshold value	4-bit DAC/channel + (3-bit + polarity bit) common DAC
Minimum threshold value	≥ noise
Readout	
Readout frequency	20 MHz to 25 MHz
Channel Readout mode	Hit channel; specific channels; all channels
SCA Readout mode	511 cells; 256 cells; 128 cells
Test	
calibration	1 channel / 72; external test capacitor
test	1 channel / 72; internal test capacitor (1/charge range)
functional	1, few or 76 channels; internal test capacitor/channel
Counting rate	
ASIC level	< 1 kHz
Power consumption	
Channel | Asic	< 10 mW / channel
Packaging	Ceramic or plastic
Temperature	ambient