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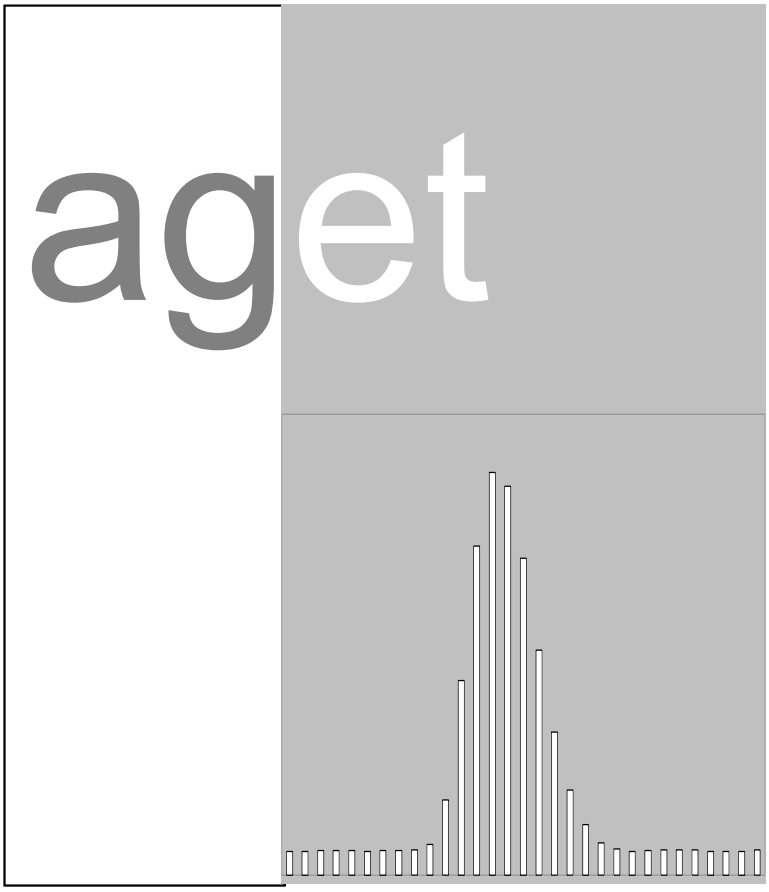
AGET, a Front End ASIC for Active Time Projection Chamber

Hit channel address & selected channel readout protocol

proposal 1.0, March 25, 2009; Author: P. Baron



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Revision history

Date	Revision	Changes
25-Mar-09	1.0	Creation

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Contents

1. Introduction

This document gives a proposal of protocol needed for the readout of the hit channel registers and used to specify the channels to be read. It is one of the last important points that it must be validated before the final design of the AGET chip.

2. General view of the architecture

The previous idea was to use the same link & protocol of the Slow Control to avoid some additional signals on the chip. But unfortunately, this solution presents some drawbacks as a lake of speed (less than 20 MHz), a length of data format not optimal (7 bits of register address before the main data) and some additional clock cycle to finish the operation.
The new solution, which is described in this document, uses always the same link (the same 4 signals) but with a simplified and fastest protocol.

2.1 Definition of the operation mode

As we use the same link, we must define an enable time window to authorize the protocol to be achieved or more precisely to disable the slow control part of the chip. It is done by considering that the operation must be done just after the SCA write phase and before the SCA read phase. Therefore, the time window will be defined on the falling edge of the SCA_write signal and will be stopped on the SCA_read signal (fig. 1).

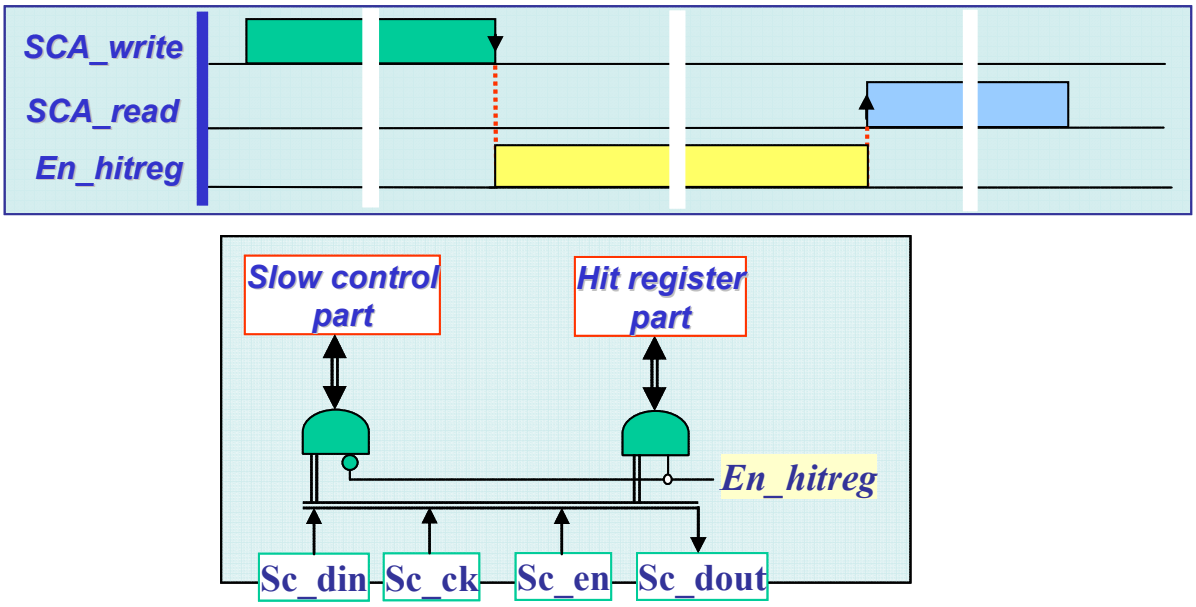

Fig 1: Definition of the operation mode.

This is a simple solution which works perfectly excepted if a SCA read phase is not achieved after the SCA write phase (event rejected after trigger criteria). In this case, it will be not possible to perform a slow control task just after because the **En_hitreg** signal will be always on (fig. 2). It will be only possible if a complete SCA operation (write & read phases) is performed, or if the SCA write or SCA read signal is on.

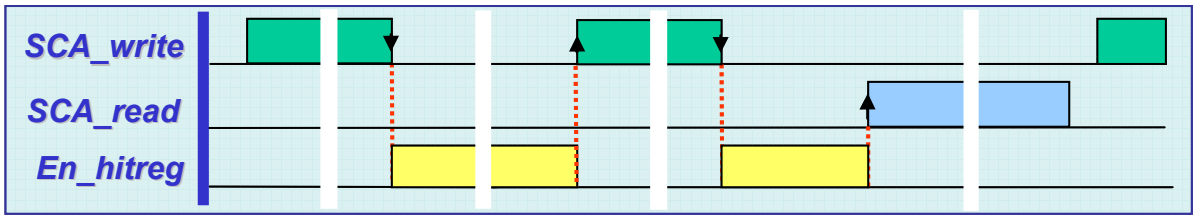

Fig 2: The operation mode in different cases.

2.2 Power on Reset

When the chip is powered on, an internal "power on reset" device delivers a reset pulse (about 1 ms of duration) resetting the hit channel register and the En_hitreg signal to "0".

2.3 Description of the slow control serial link

The link uses **4** signals:

- ***Sc_din***: input data of the serial link.
- ***Sc_ck:*** clock of the serial link.
- ***Sc_en***: enable of the serial link.
- ***Sc_dout:*** output data of the serial link.

The signals ***Sc_din*** & ***Sc_en*** must be synchronous to the rising edge of ***Sc_ck.*** The data are sampled on the input lines, decoded and operations of reading/writing are carried out, by the asic, on the rising edge of ***Sc_ck***. Thus, the data at the output of ***Sc_dout*** will be synchronous on this edge.
On ***Sc_din,*** the first bit [r/wb] defines the type of operation. **r/wb** =1 for the readout and **r/wb** =0 for the write.
The ***Sc_en*** signal frames the data sent on ***Sc_din*** or read on ***Sc_dout***. It must go up simultaneously with the positioning of [**r/wb**] and must go down on the rising edge of ***Sc_ck*** after the positioning of the last bit of data on ***Sc_din*** or on ***Sc_dout***. Thus, the data packet defined by the setting of the ***Sc_en*** signal to "1" must frame **77** of ***Sc_ck*** clock cycle.
Between the slow-control frames, the ***Sc_dout*** output is in high impedance state (HZ).

2.4 Write mode [writing of the read channel address]

The write mode (fig. 3) is defined by the first bit **r/wb = 0** on ***Sc_din***. On the seventy-eighth rising edge of ***Sc_ck***, the read address channel is written in the different registers (internal operation by using counter). During **76** clocks, ***Sc_dout*** takes the states of the hit channel registers, according to the history, and will come back to its high impedance state (HZ) after the falling of ***Sc_en.***

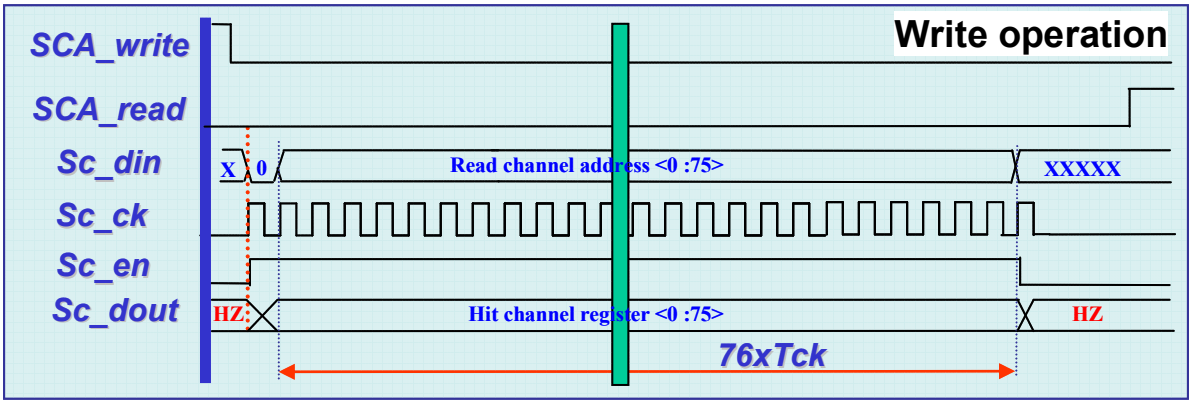

Fig 3: The writing mode operation.

2.5 Read mode [read of the hit channel address]

The read mode (fig. 4) is defined by the first bit **r/wb = 1** on ***Sc_din***. On the seventy-seventh rising edge of ***Sc_ck***, the last bit of the hit channel registers (corresponding of the channel 75) is put on the ***Sc_dout***. The read mode is achieved on the next rising edge of the ***Sc_ck,*** and ***Sc_dout*** go back to the high impedance state.

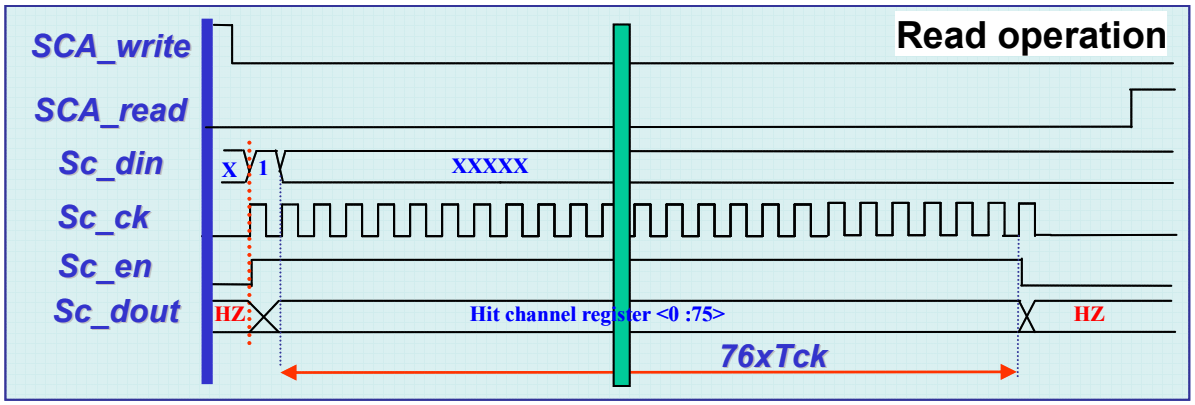

Fig 4: The read mode operation.

2.6 Timing specifications

A first level of simulation has been made. The specification of 50 MHz asked for the clock frequency can be reached with a safety margin (it works also at 100 MHz).