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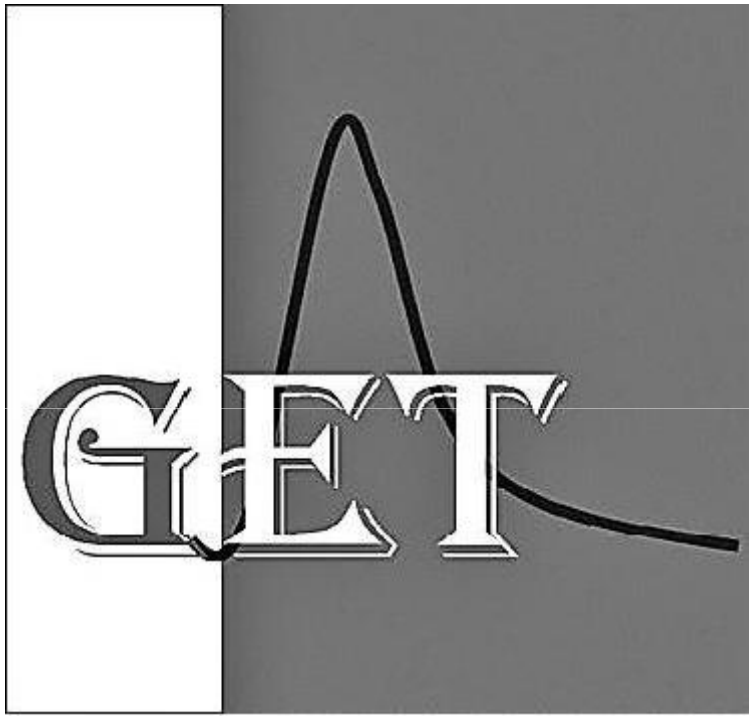
The AGET chip

Architecture, Design & Status



Technical Workshop

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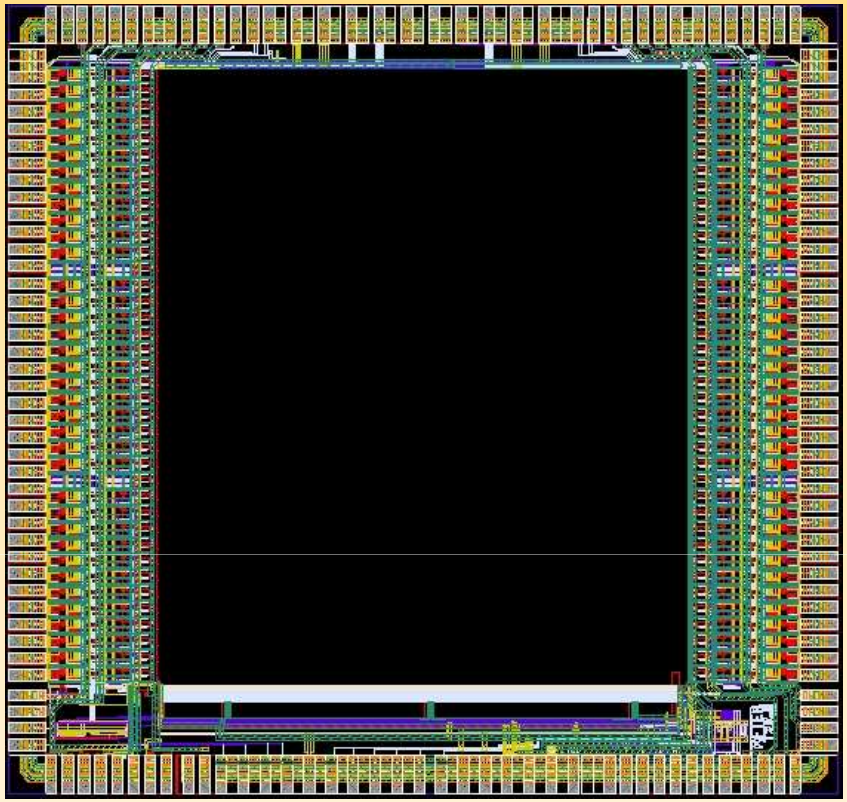
Outline

- *Architecture,*
- *Design,*
- *Status.*



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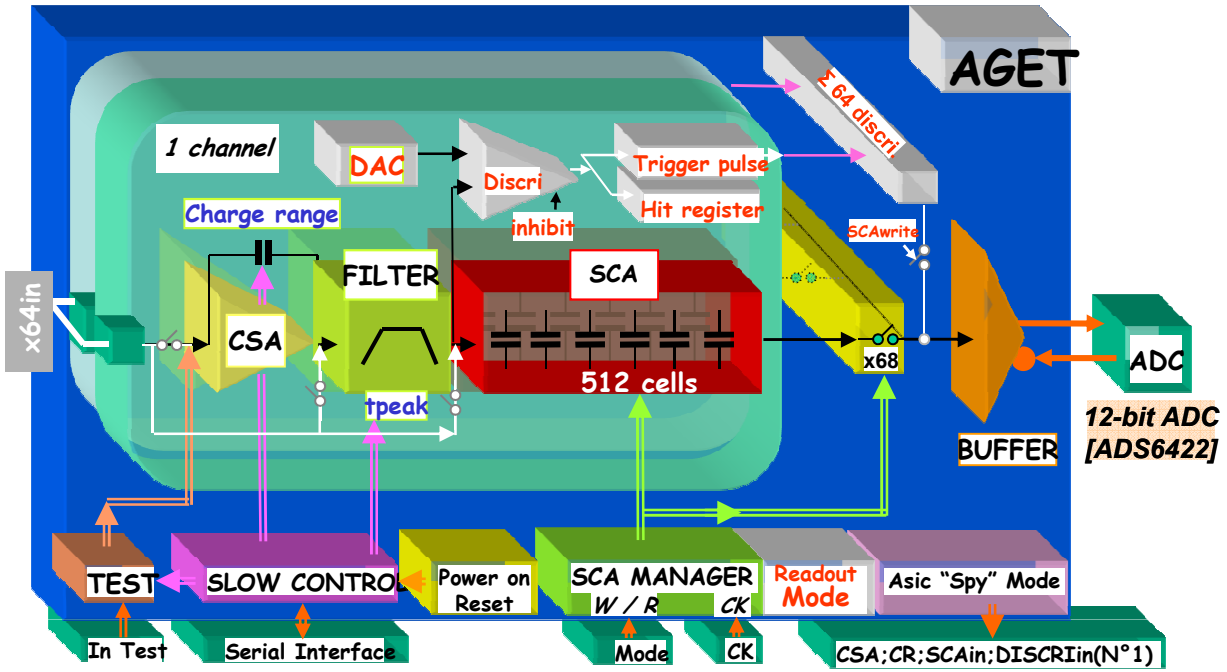
AGET: Architecture



Main features for AGET

- 64 Analog Channels: Analog part + Sampling Capacitor Array.

Main features for the channel

- CSA + PZC + Filter (semi-Gaussian order 2).
- SCA: 512 analog memory cells.
- Auto Triggering: discriminator + threshold (DAC) + inhibition.

Main features for the readout

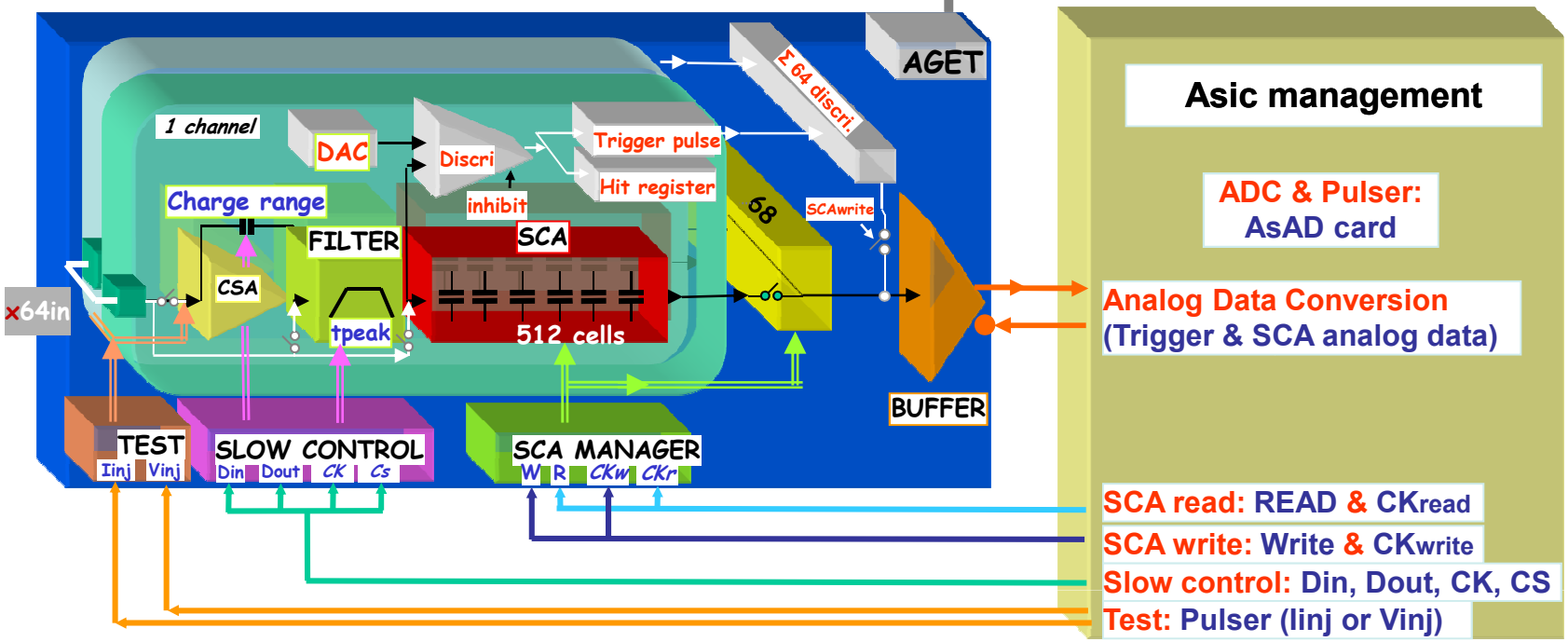
- Trigger [Analog sum of the 64 discri.].
- Several SCA readout modes.
- Address of the hit channel(s) [read & write].

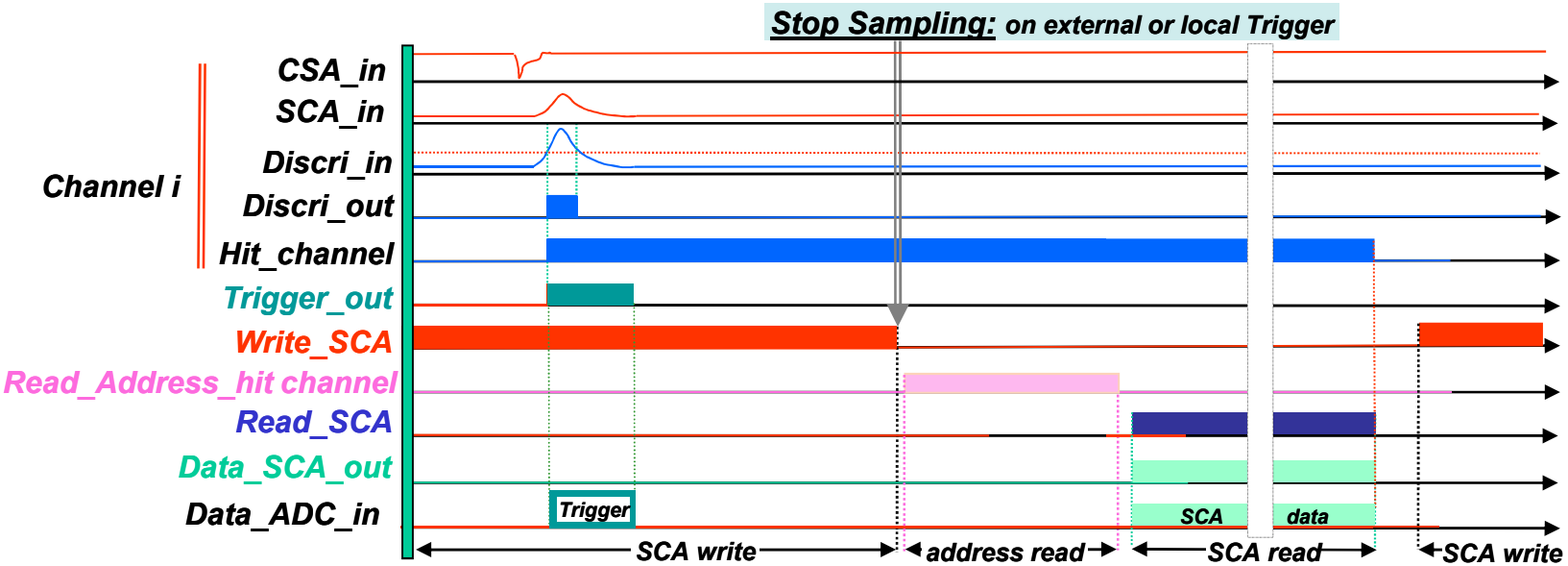
Ion & radioactivity acquisition case:

- *SCA split in two independent memories.*

- Slow Control.
- Power on reset.
- Test mode:
  calibration or test
  [channel/channel]
  functional
  [all channels on one shot]
- Spy mode (cx 1).

AGET: Mode of operation





AGET: Charge Channel

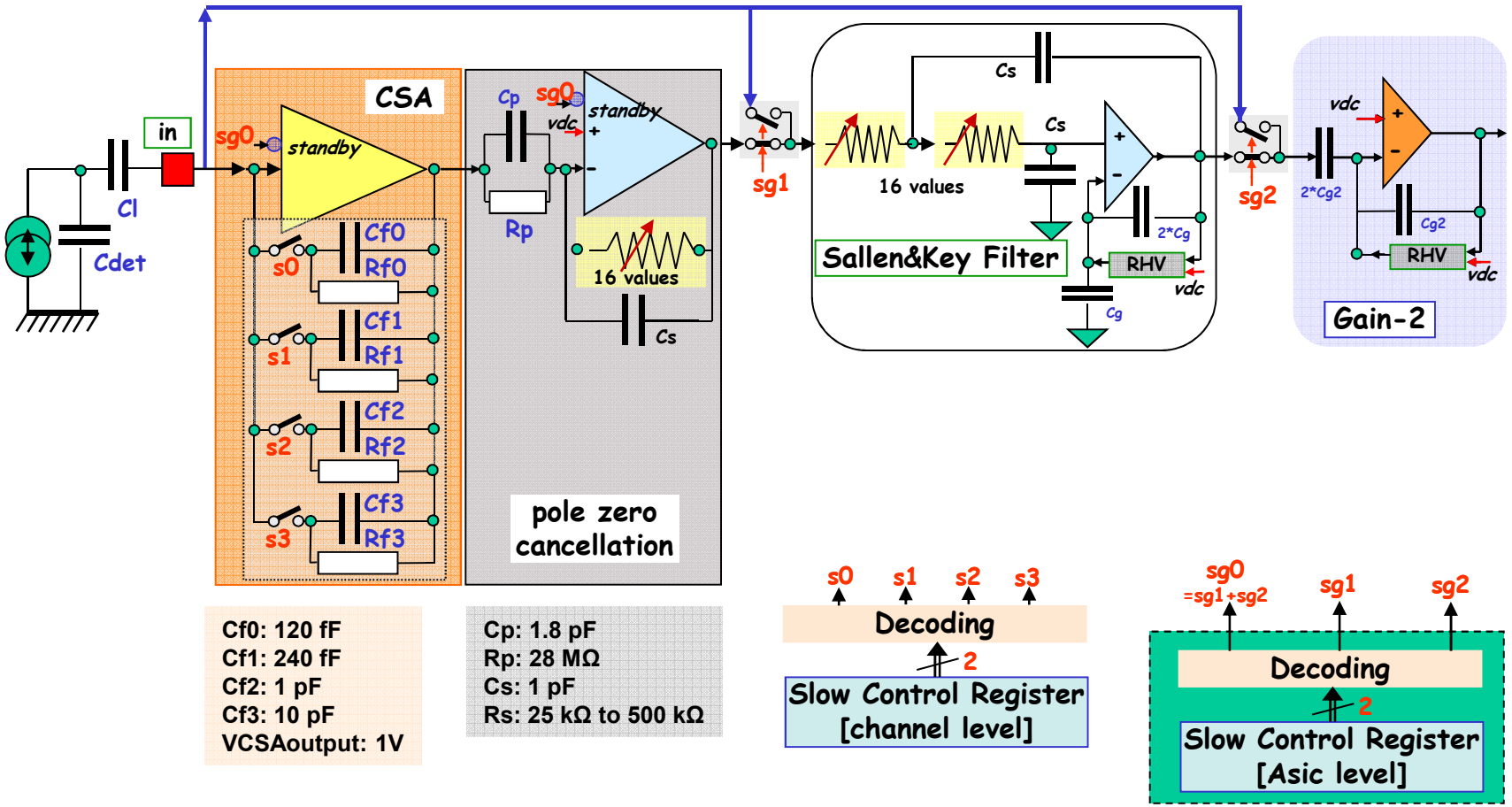
CSA level: **4 Charge ranges; 2 bits register / channel: 120 fC, 240 fC, 1 pC & 10 pC.**

PZC level: **zero: 50 µs; Pole: 25ns to 500ns.**

RC2 level: **Pole: 25 ns to 500 ns.**

Bypass: **[CSA+PZC] or [CSA+PZC+RC2]; 2 global register bits.**

Peaking Time: **50ns to 1µs**



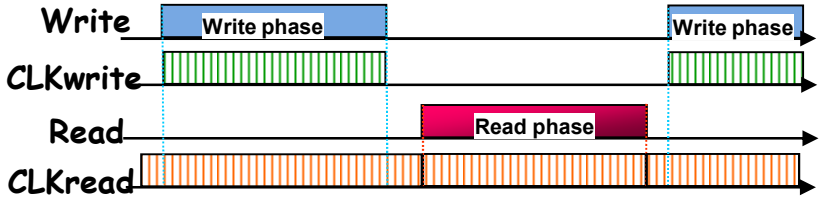
AGET: SCA

***SCA:* Circular Memory**

64 channels + 4 dummy channels

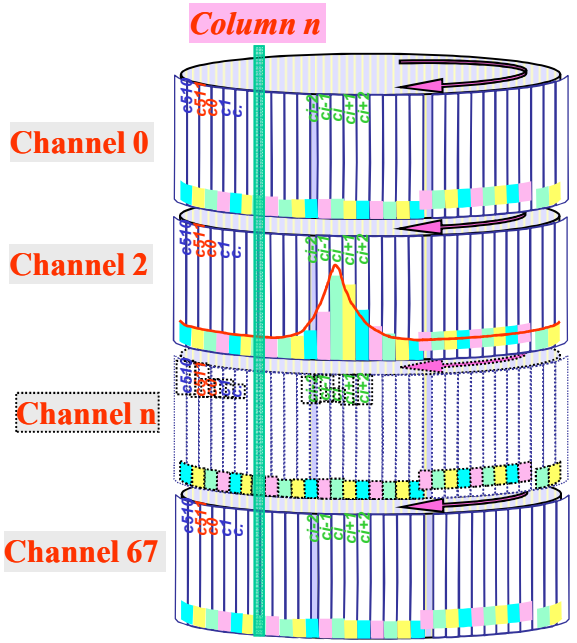
[for common mode or Fix pattern noise rejection purpose].

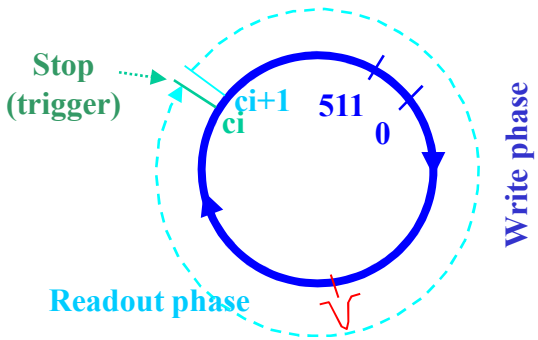
- **Write: 1MHz to 100MHz**
- **Read: 25MHz**



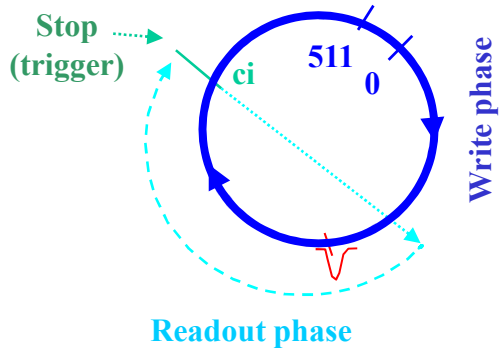
SCA readout mode:

512, 256 or 128 analog memory cells / channel

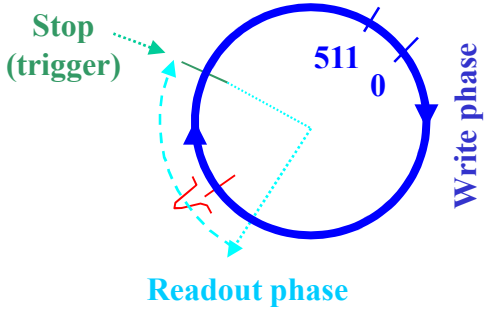




Write phase:
Tdrift ≤ 512 / Fsampling
Read phase:
SCAcells = 512



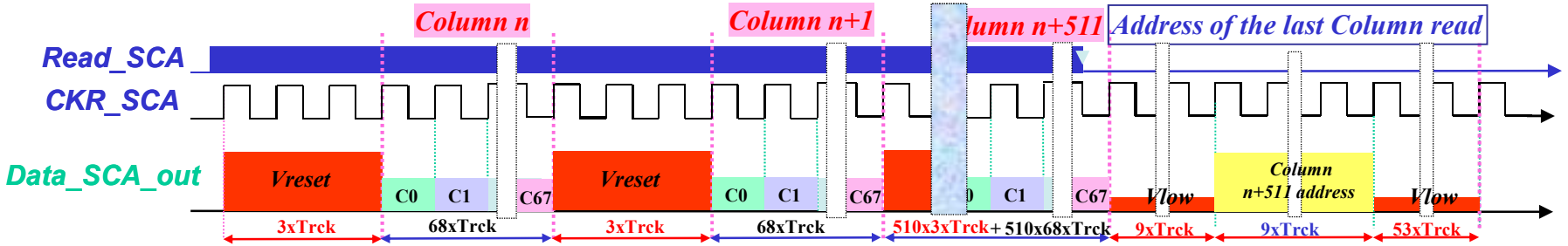
Write phase:
2 x Tdrift ≤ 512 / Fsampling
Read phase:
SCAcells = 256



Write phase:
4 x Tdrift ≤ 512 / Fsampling
Read phase:
SCAcells = 128

AGET: SCA

Channel readout mode: **all, hit or specific channels.**



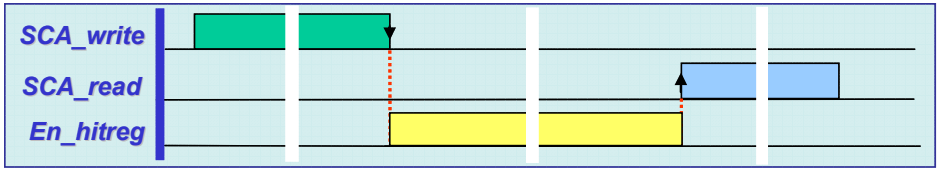
SCA readout time: m memory cell x [n channel + 3] xTrck + 71 x Trck. [Trck = 40 ns]

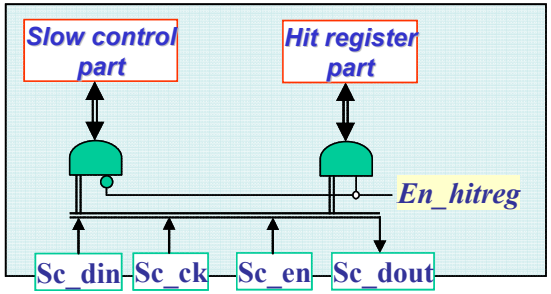
Channel number	SCA = 512 cells	SCA = 256 cells	SCA = 128 cells
1	84.76 µs	43.80 µs	23.32 µs
10	269.08 µs	135.96 µs	69.40 µs
32	719.08 µs	361.24 µs	182.04 µs
64	1375 µs	688.92 µs	345.88 µs
68	1457 µs	729.88 µs	366.36 µs

AGET: SCA

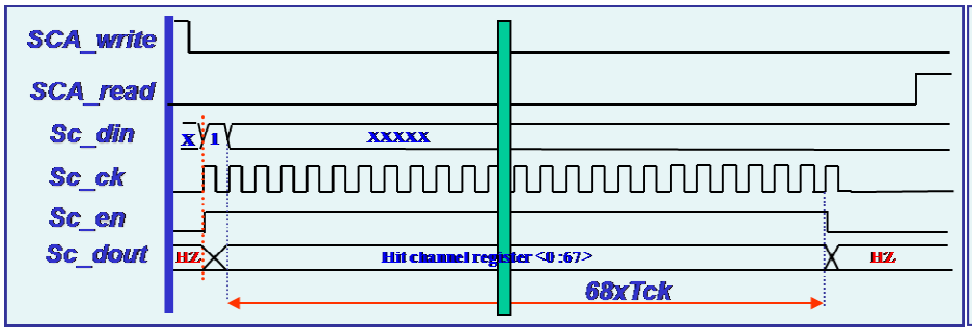
Hit channel address & selected channel readout protocol:

The same link as the one for the "slow" control, with a "simplified" & fastest protocol [50 MHz].

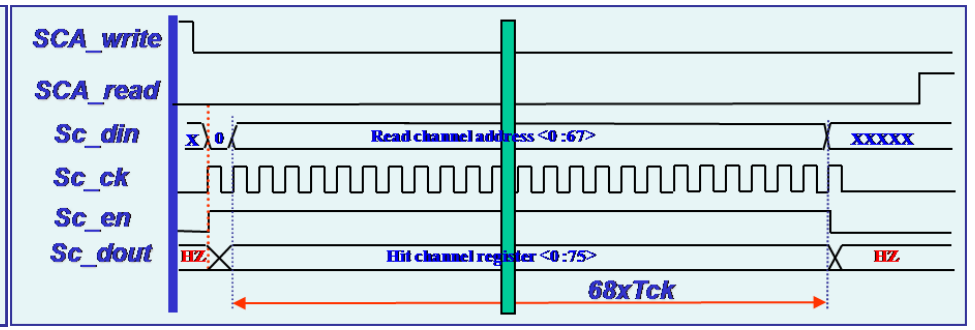




Read mode:



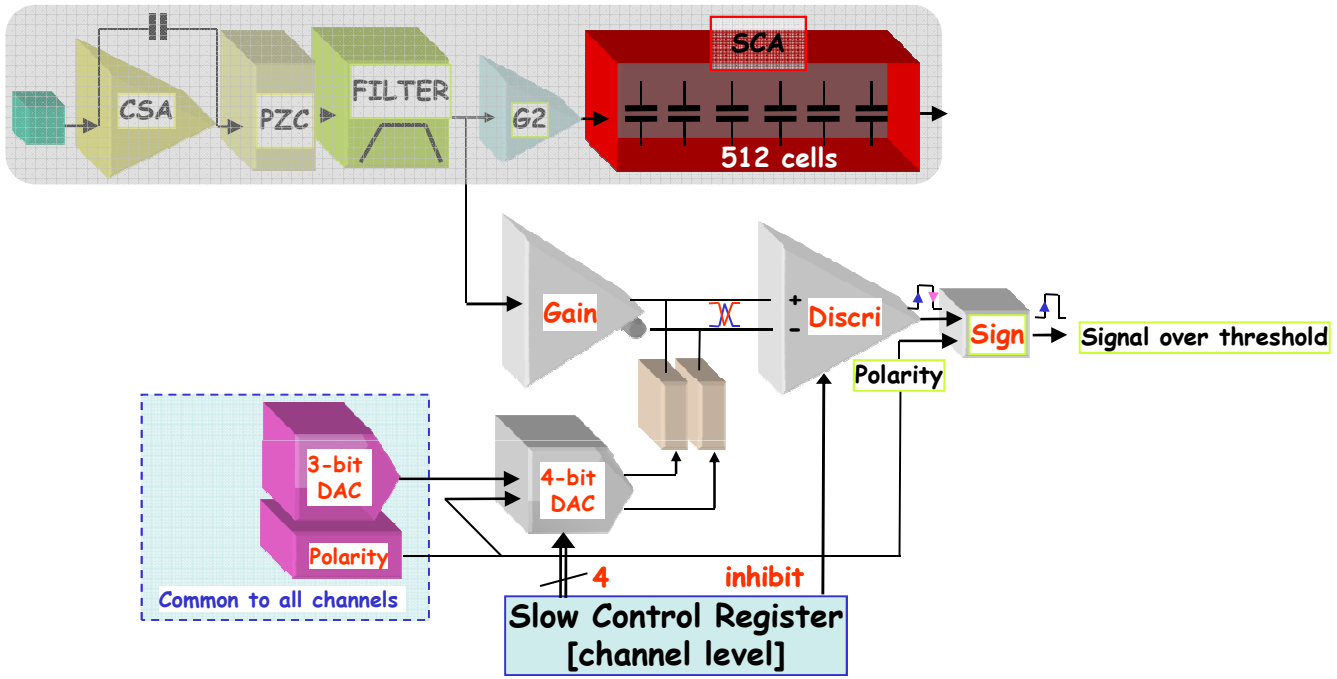
Write mode:



AGET: Trigger channel

Differential gain stage + discriminator + dac + logic & register:

Threshold value: ***Tunable; Global DAC [3 bits + polarity bit] + individual DAC [4 bits]***



Signal over threshold **=> Trigger signal & memory in hit channel register**

AGET: Trigger channel

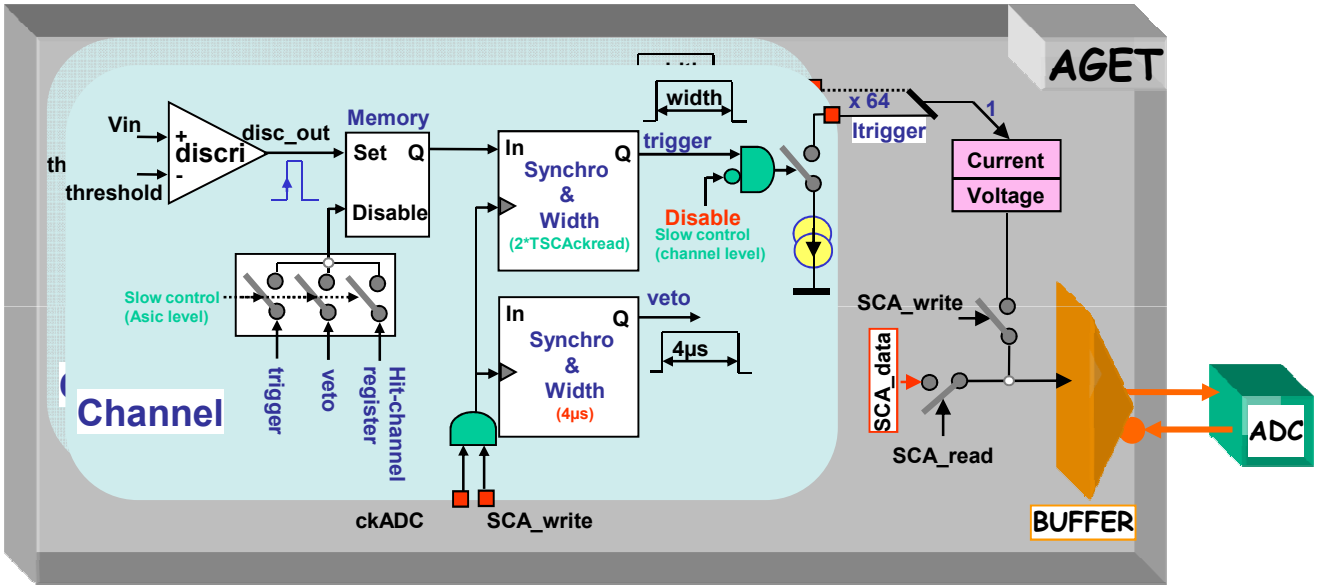
Trigger architecture: ***analog sum of the 64 discriminators outputs***

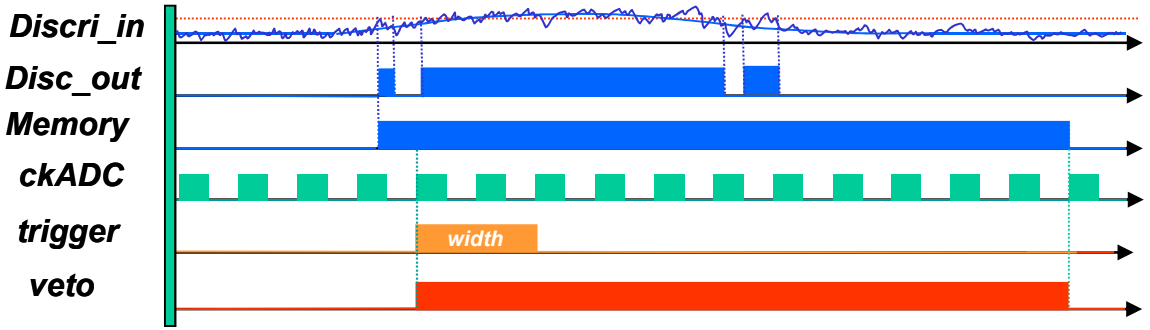
Signal: ***synchronous of the SCA readout clock (CKADC).***

Width: ***2 x TCKADC.***

Veto [to avoid ringing]: ***any, fixed value (4µs +/- 1.5µs) or hit-channel register.***

Disable [to avoid beam contribution]: ***by slow control.***





AGET: Hit channel register

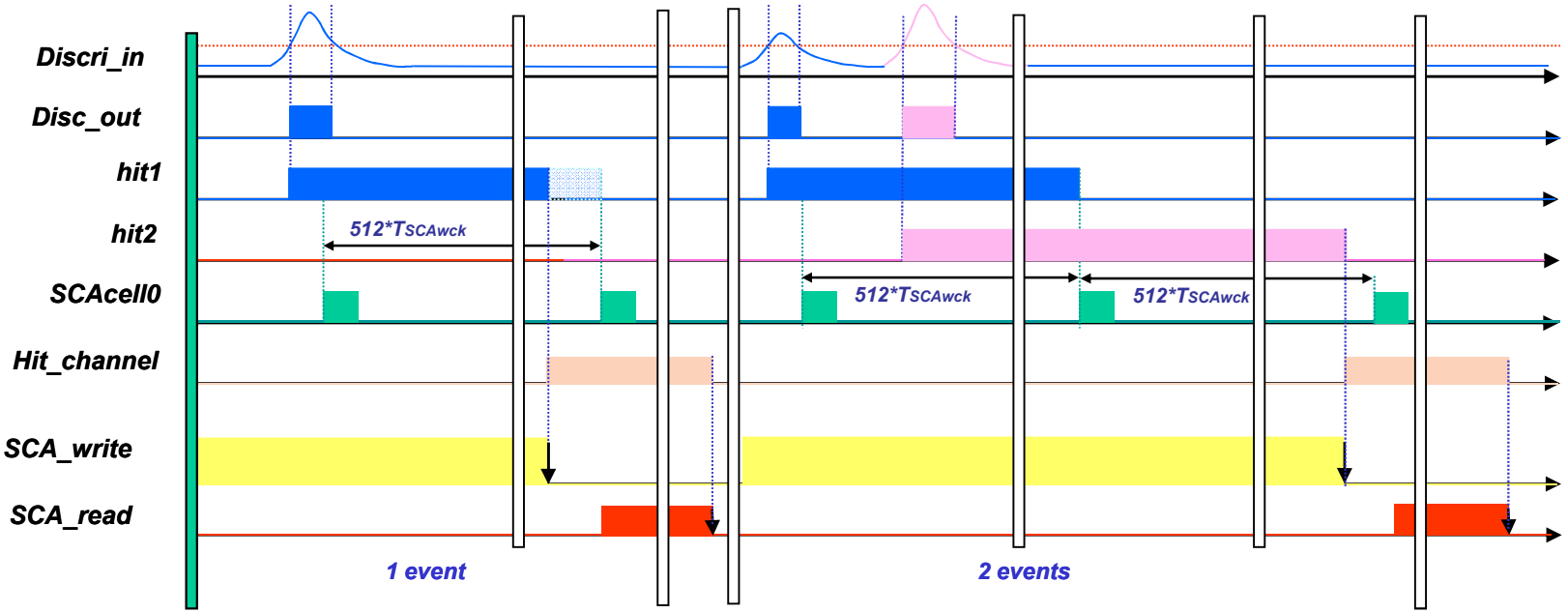
Hit channel register:

Signal: ***synchronous of the discriminator output***

Width: ***1 to 2 complete SCA sampling time.***

Enable: ***on the falling edge of the SCA write signal.***

Multiple hit event: ***2 [the width is extended to 1 complete SCA sampling time].***

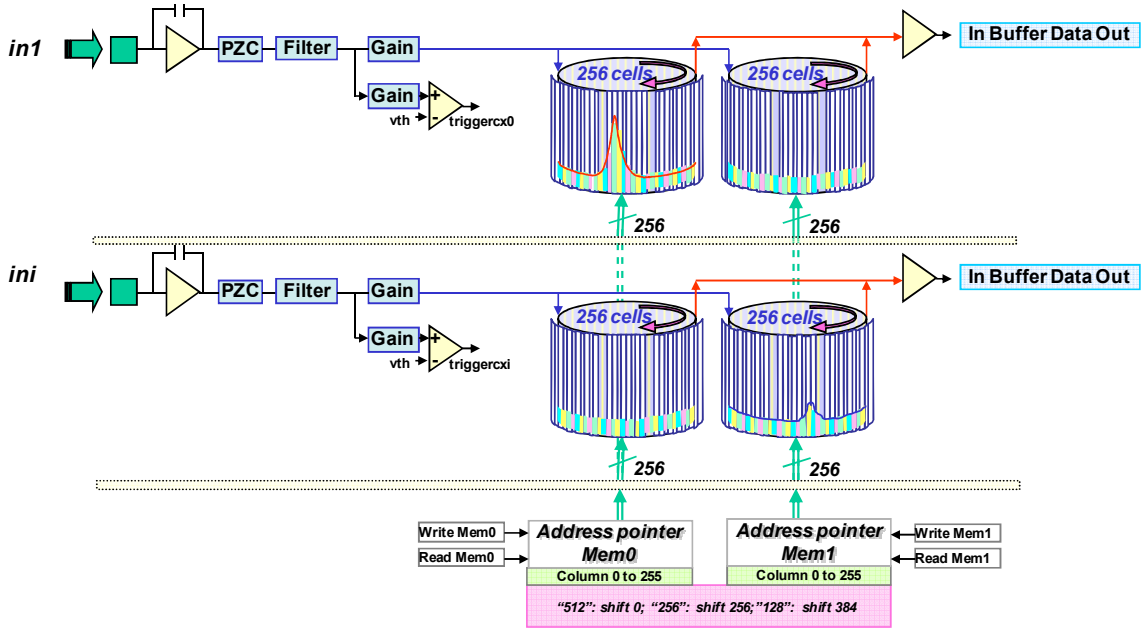


AGET: ion & radioactivity acquisition case

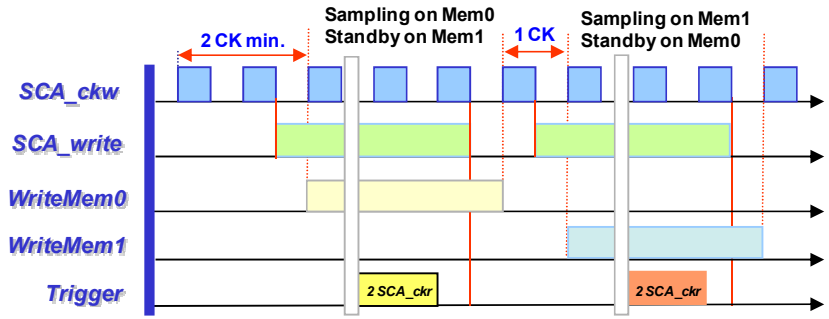
Goal: ***ability to sample and store 2 consecutive events.***

Architecture: **the SCA is splitting in two separate memories of 256 cells.**

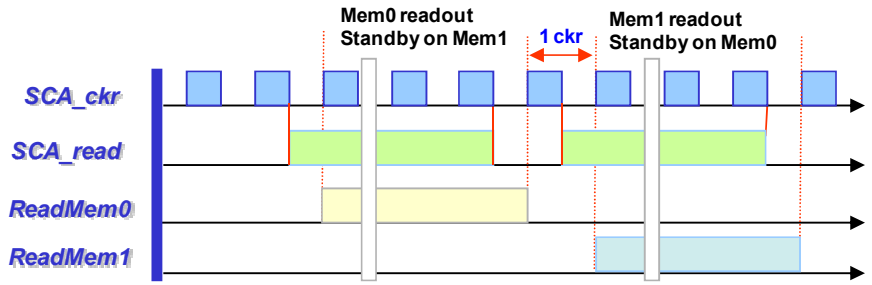
Hit channel register: **1 for the 2 memories ["OR" of the 2 events].**



Write phase



Read phase



AGET: Slow control

Serial protocol

Format: [r/wb] [Ad_6 … Ad_0][D_{NBD-1} …D_0]

4 signals:

Din: input data; Dout: output data; Ck: clock; Cs: enable

Preliminary !!

address	name	width	access	action
0	**dummy**		W	used to test the serial link
1	**ASIC configuration 1**	32 bits	R/W	chip configuration
2	**ASIC configuration 2**	16 bits	R/W	special modes and test config.
3	**First group test selection**	34 bits	R/W	selection of tested channels
4	**Second group test selection**	34 bits	R/W	selection of tested channels
5	**ASIC version number**	16 bits	R	Contains the version number of the chip
6	**Gain 1 to 32**	64 bits	R/W	Input charge range of the channel 1 to 32
7	**Gain 33 to 64**	64 bits	R/W	Input charge range of the channel 33 to 64
8	**threshold 1 to 32**	128 bits	R/W	threshold of the channel 1 to 32
9	**threshold 33 to 64**	128 bits	R/W	threshold of the channel 33 to 64
10	**Inhibition 1 to 32**	64 bits	R/W	inhibition of the channel 1 to 32
11	**inhibition 33 to 64**	64 bits	R/W	inhibition of the channel 33 to 64

Mapping of the AGET slow-control registers

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AGET: Requirements

Parameter	Value
Polarity of detector signal	Negative or Positive
Number of channels	64
External Preamplifier	Yes; access to the filter or SCA inputs
Charge measurement	
Input dynamic range	120 fC; 240 fC; 1 pC; 10 pC
Gain	Adjustable/(channel)
Output dynamic range	2V p-p
I.N.L	< 2%
Resolution	< 850 e- (Charge range: 120fC; Peaking Time: 200ns; Cinchannel. < 30pF)
Sampling	
Peaking time value	50 ns to 1 µs (16 values)
Number of SCA Time bins	512
Sampling Frequency	1 MHz to 100 MHz
Time resolution	
Jitter	60 ps rms
Skew	< 700 ps rms
Trigger	
Discriminator solution	L.E.D
Trigger Output/Multiplicity	OR of the 64 discriminator outputs (pulse of 2*TckADC)
Dynamic range	5% of input charge range
I.N.L	< 5%
Threshold value	4-bit DAC/channel + (3-bit + polarity bit) common DAC
Minimum threshold value	≥ noise
Readout	
Readout frequency	25 MHz
Channel Readout mode	Hit channel; specific channels; all channels
SCA Readout mode	512 cells; 256 cells; 128 cells
Test	
calibration	1 channel / 64; external test capacitor
test	1 channel / 64; internal test capacitor (1/charge range)
functional	1, few or 68 channels; internal test capacitor/channel
Counting rate	< 1 kHz
Power consumption	< 10 mW / channel

AGET: Status

Design of the chip:

Analog part of the channel: **complete (98%).**

Threshold DAC; reference voltage & current sources; debug bloc; Test bloc: **complete (100%)**

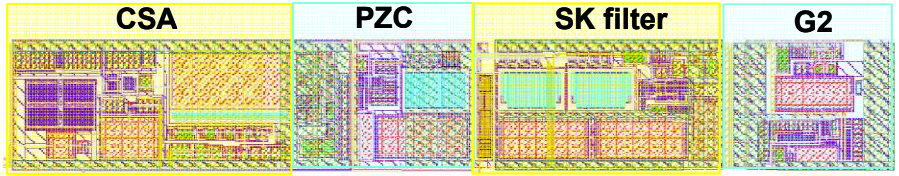
SCA: ***in progress.***

Hit register/write phase/readout phase/ion&radioactivity events: ***must be finalized.***

Layout of the Analog channel

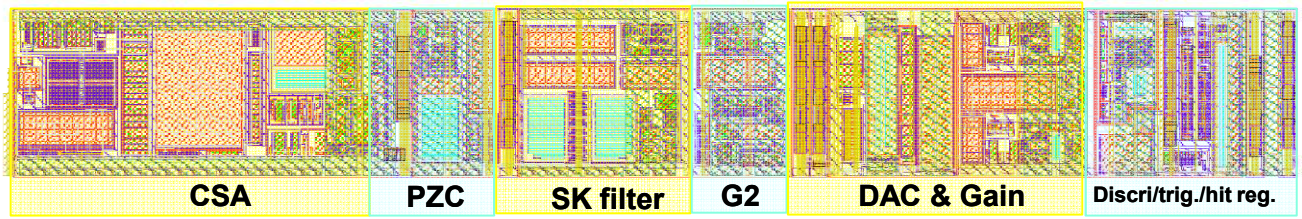
AFTER

[963 µmx140 µm]



AGET

[1400 µmx183 µm]



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AGET: Schedule

AMS technology run schedule:

7 December 2009: not ready.

5 February 2010: new time target.

21 May, 9 July, 27 August & 3 December 2010: *other runs of the 2010 year.*

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Conclusion

- ***Not ready for the submission of December 2009***
- ***Submission for February 2010 could be foreseen.***