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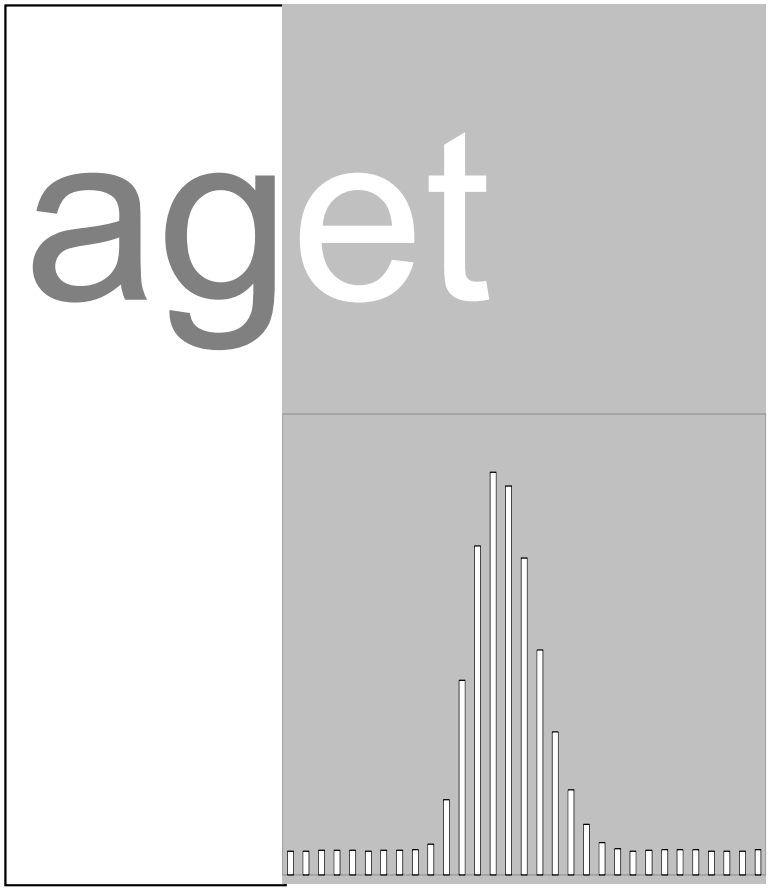
AGET, a Front End ASIC for Active Time Projection Chamber

Proposal for the readout of two consecutive events

proposal 1.0, April 7, 2009; Author: P. Baron & E. Delagnes



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Revision history

Date	Revision	Changes
7-April-09	1.0	Creation

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Contents

1. Introduction

This document gives a proposal of architecture for the processing of two consecutive events in a time window less than 1 or 2 ms corresponding to the typical event (implantation & decay) studied by the CENBG team.

2. General view of the architecture

The architecture of the AGET chip does not allow the processing of a second event during the SCA readout of the previous event. This dead time is proportional to the number of channel and memory cells read, and can be optimized by reading only the hit channels and by limiting the depth of the SCA (256 or 128). To avoid this dead time which is necessary to read the event, the idea is to perform the global readout after that the first and the second event have been sampled and stored in the SCA. This is possible by splitting the SCA in two separate memories of 256 cells. This configuration will be programmable by a Slow Control bit.

2.1 Structure of the SCA & description of the write and read phases

The SCA (fig. 1) is divided in two separate memories: Mem0 and Mem1. Each memory has its own address pointer in write and read phases.

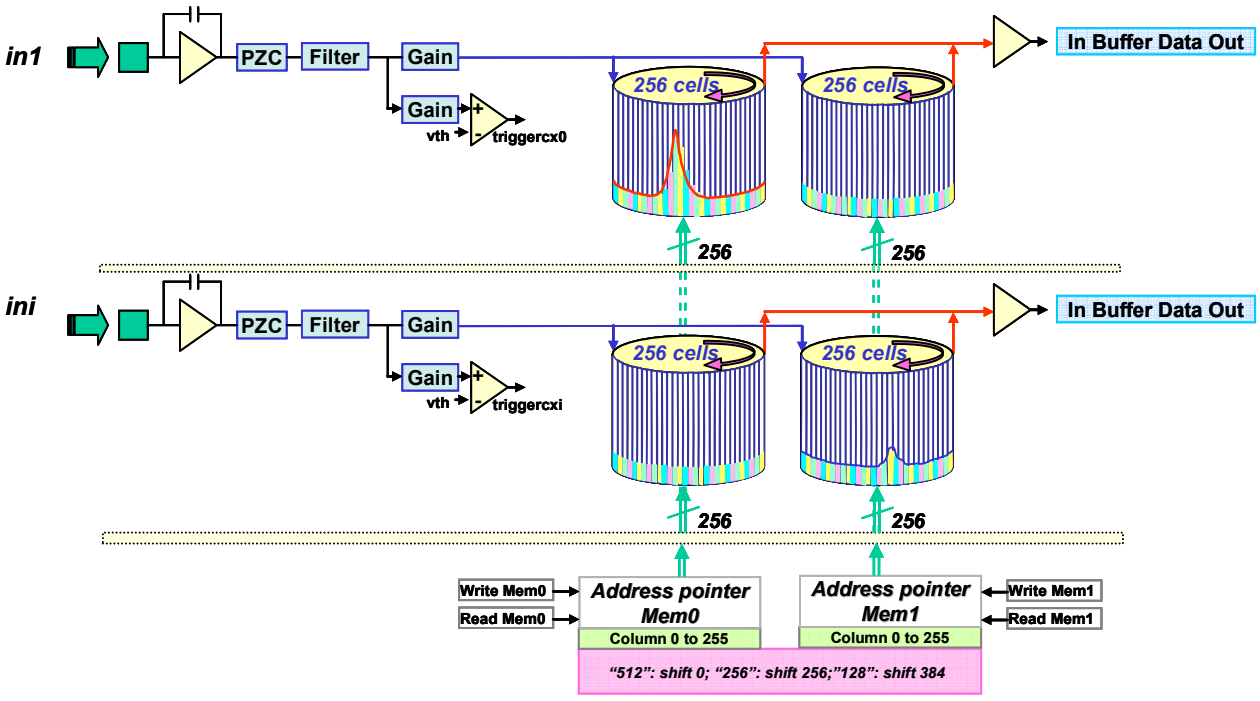

Fig 1: Structure of the SCA.

In the write phase (fig. 2), the analog signal of each channel is sampled and stored in the Mem0. On a trigger, the sampling in Mem0 is stopped on the falling edge of the SCA write signal (SCA_write). The sampling will be also authorized and performed on the Mem1 and not on Mem0 after one period of the SCA clock (SCA_ckw) and on the leading edge of the next SCA write signal. This sampling on Mem1 is stopped on the falling edge of SCA_write.

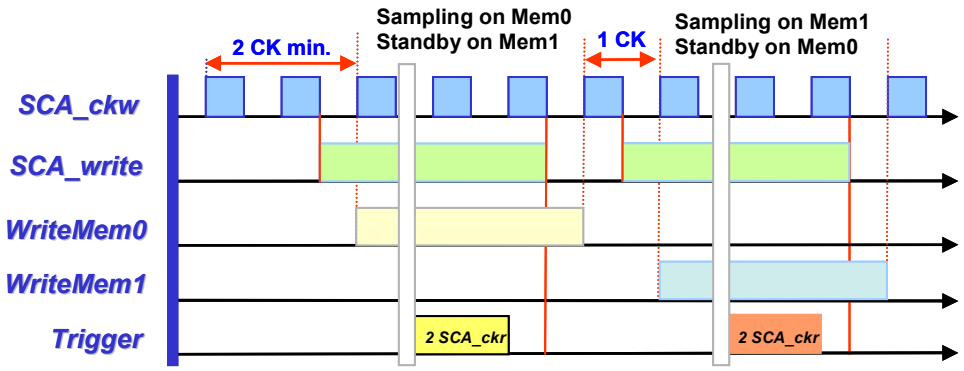

Fig 2: The write operation.

For the read phase (fig. 3), the same methodology is used by starting firstly with the Mem0 readout and secondly with the Mem1 readout. The readout of the two memories is managed by the SCA read clock signal (SCA_ckr) and by the SCA read signal (SCA_read).

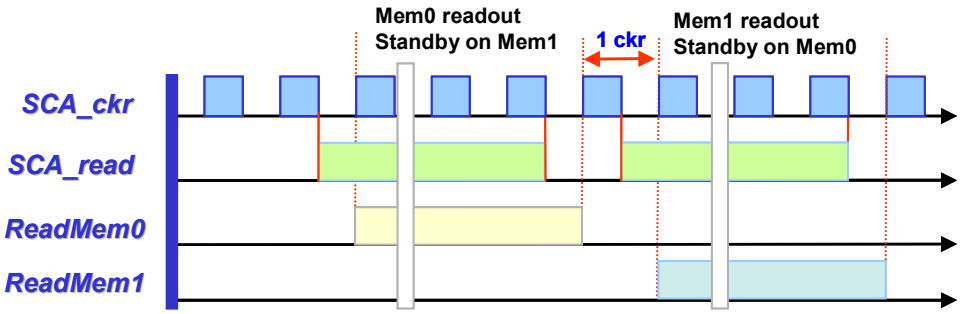

Fig 3: The read operation.

2.2 Hit channel register and selected channel readout

For the trigger part of the channel, it works as in a nominal mode. If the signal is higher than the threshold value, it gives an individual Trigger of 2xTSCA_ckr width. If the channel is hit by the 2 consecutive events, it gives 2 trigger pulses. For the hit channel register, some parameters are changing.
The memory time of the signal corresponds always to a value comprise between 1 and 2 SCA write cycle, but with a SCA write cycle equal to 256 cells.
For the hit channel register itself, there are 2 possibilities:

- The first is to have only one register for the 2 events. This register is put “on” if on one of the two falling edges of the SCA write signal, the memory time of the signal is active. The advantage is to have only one register and therefore to have only 76 register bits to read through the “fast slow” control link (fig. 4). The drawback is to have a data read time not optimal (if a channel is hit by only one event, its two memories will be read instead of one).

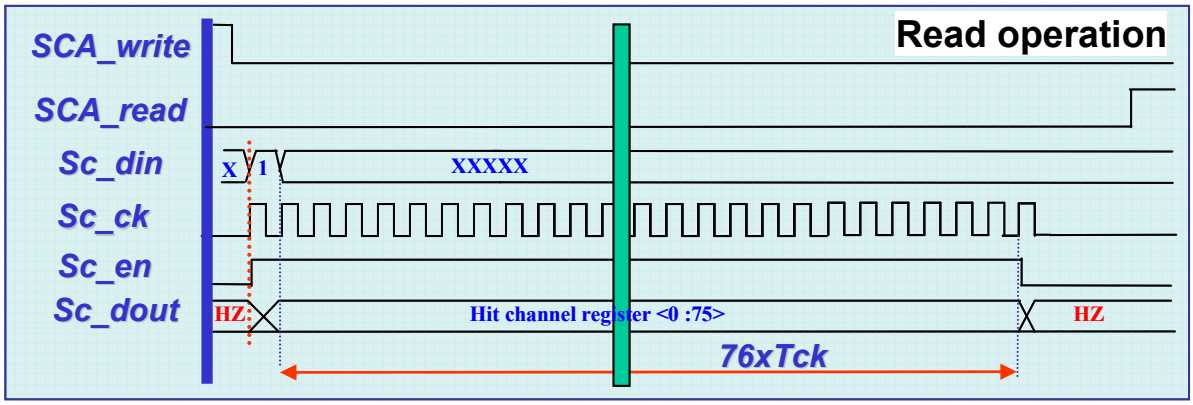

Fig 4: The hit channel register read operation with 1 register.

- The second is to have one register for each event (2 registers). Each register is put “on” if on the falling edge of the corresponding SCA write signal, the memory time of the signal is active. The advantage is to have a read time optimized (we read only the memory which contains the data). The drawback is to have 152 register bits to read or to write (fig. 5).

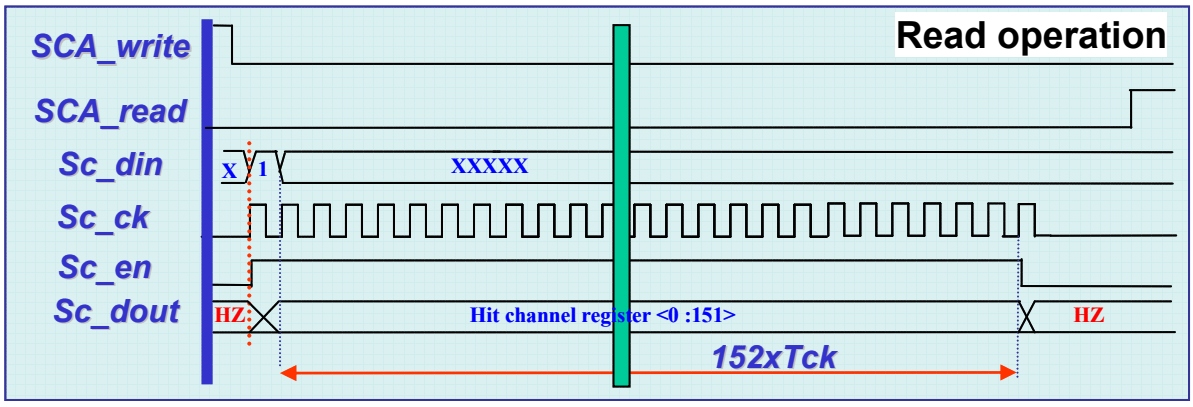

Fig 5: The hit channel register read operation with 2 registers.

Conclusion

The solution presented in this document seems to be adapted for the treatment of the 2p events or for other consecutive events. Its design concerns principally some changes and additional logic on the management of the memory address pointer and seems realizable. For the hit channel register, it is clear that to have 2 registers per channel will be better for the global dead time, but if someone claims the contrary, the writer of this document (who is also designer of the chip) will agree with him (in quite objectively ...).