Commissariat à l'énergie atomique
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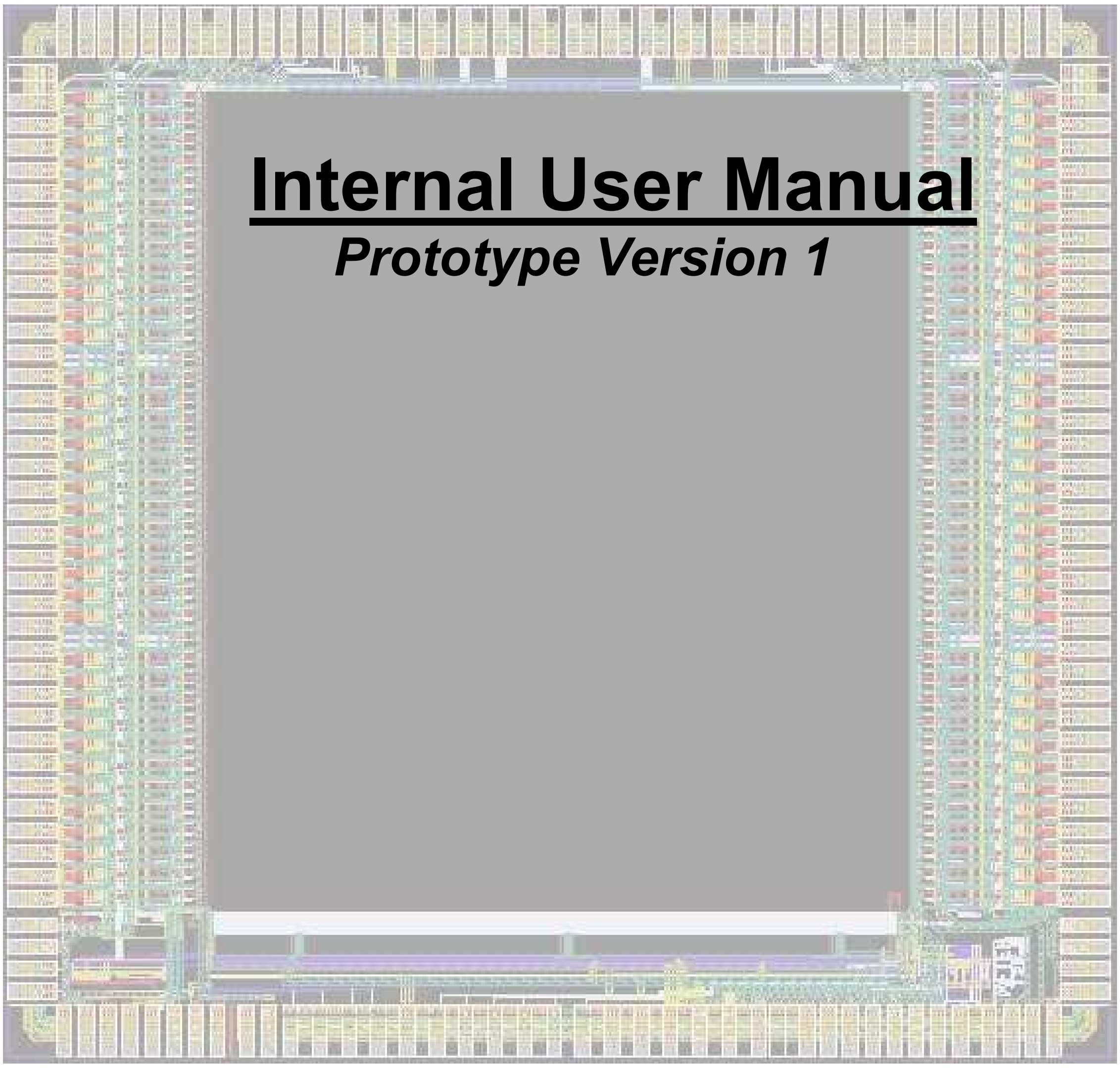
ASIC AFTER



Internal User Manual

Prototype Version 1

This document gives a detailed description of the chip AFTER, and presents the main performances expected. It is an internal document specially dedicated to the test of the first prototype and therefore could be subject at some modifications if necessary.

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1 Introduction

The ***AFTER*** (**A**sic **F**or **T**PC **E**lectronic **R**ead out) chip is designed to the processing of signals coming from the module of the **T**ime **P**rojection **C**hamber. This module (Fig.1) has its electronic localized on 2 cards: ***FEC*** & ***FEM***.

F.E.C (**F**ront end **E**lectronic **C**ard): This card contains 4 asic AFTER with a Quad Channel ADC. This card is plugged directly on the module through 4 connectors. Each asic has its 72 inputs connected to one of these connectors. Its analog output is digitized on one of the ADC input. All the components on the FEC are controlled by the FEM. A total of 6 FEC is needed for the equipment of one module.

F.E.M (**F**ront **E**nd **M**ezzanine): This card controls the 6 FECs of the module, and is connected to them through individual connectors. The interface transports fast LVDS signals (up to 120 MHz DDR), skew, jitter and latency critical signals (ADC and SCA clock and timing signals) and slow control signals. The readout data of the module are transmitted to the Digital Concentrator Card (The DCC is outside of the magnet) through an Optical Transceiver.

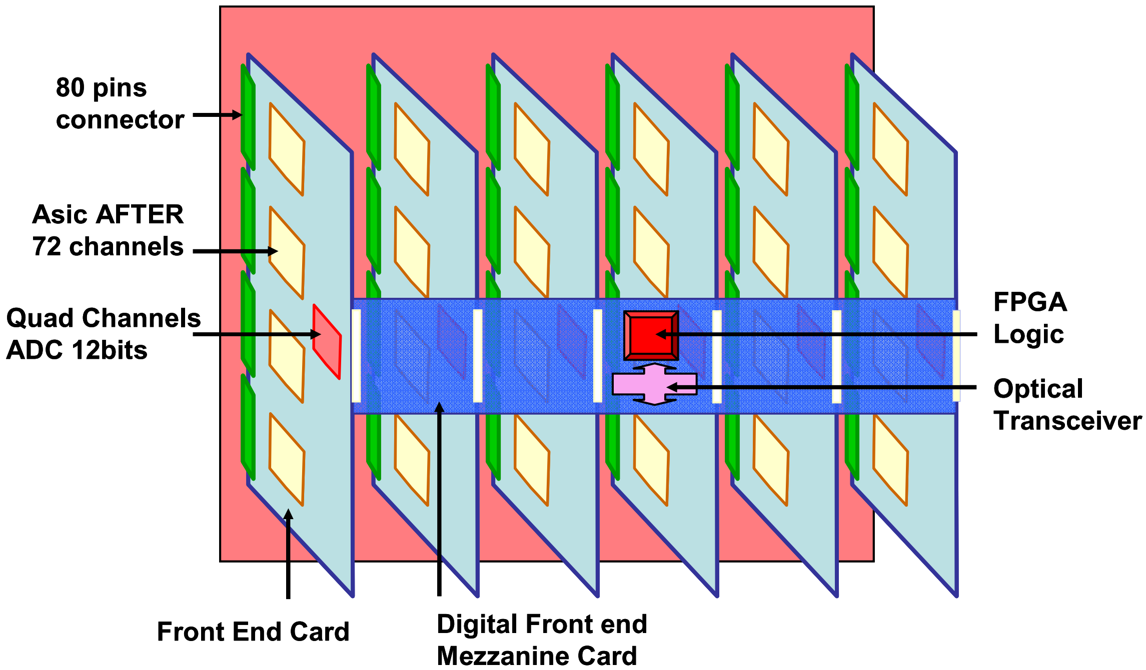


Fig.1: electronic of one TPC module

This asic ***AFTER*** contains **72** individual channels (Fig.2) handling each one detector pad. A channel integrates: charge sensitive preamplifier, analog filter (shaper) and a 511 point analog memory. This memory is based on the **S**witched **C**apacitor **A**rray structure (**SCA**), and used as a circular buffer in which the analog signal coming out from the shaper is continuously sampled and stored. The sampling is stopped when an external Trigger arrived on the TPC **F**ront **E**nd **M**ezzanine (**F.E.M**). Then, the 511 samples of each channel are read back, starting by the oldest sample. The analog data are time domain multiplexed and read toward a single external 12 bits ADC channel.

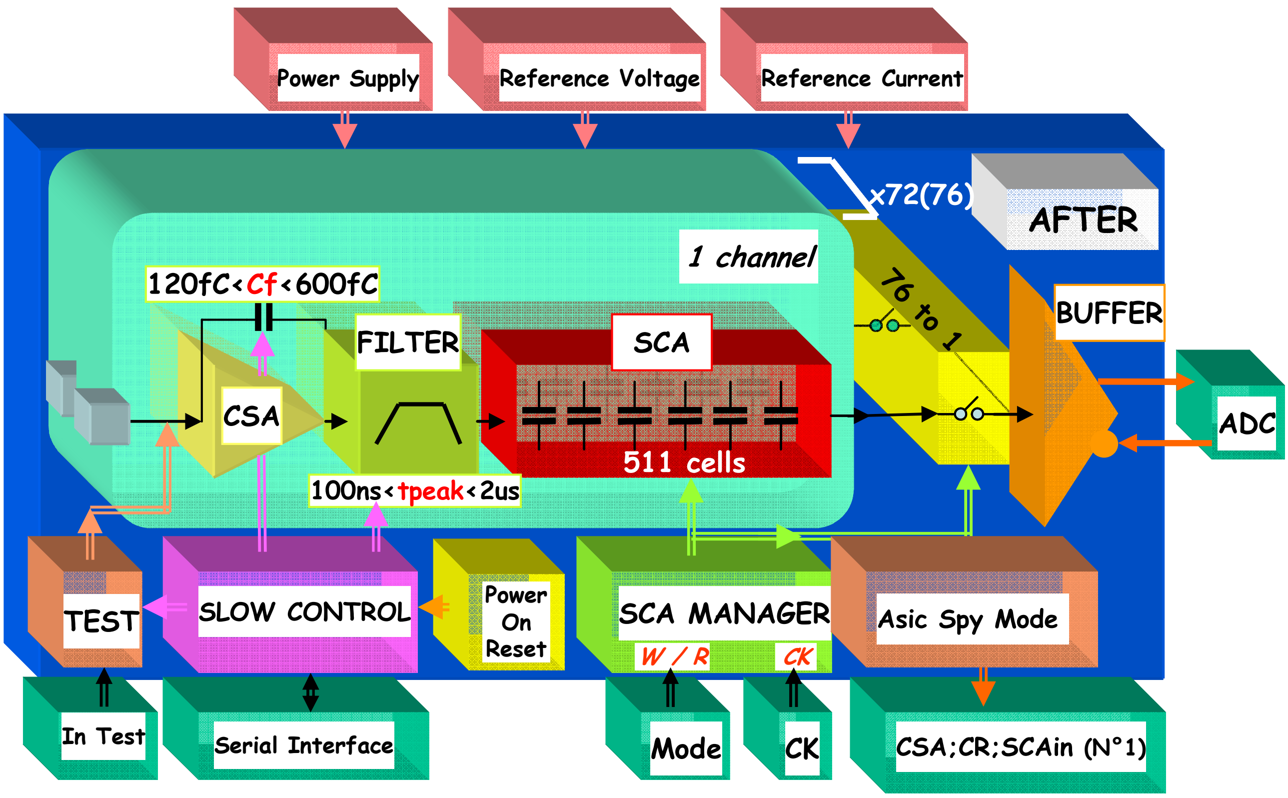


Fig.2: Architecture of AFTER chip

The global parameters (gain, peaking time, test mode and asic control) are managed by Slow Control, for which a serial protocol is used. Two inputs allow the possibility to calibrate or to test the 72 channels. A "spy" mode will be helpful to control some internal points (CSA & CR outputs and SCA input) of the analog channel number 1.

The design of the chip AFTER must satisfy the requirements and the TPC specifications defined in the beginning of the 2005 (table 1).

Parameter	**Value**
Number of channels	*72*
Number of Time bins	*511*
MIP	*12fC to 60fC*
MIP/noise	*100*
Dynamic range	*10 MIPS on 12bits*
I.N.L	*1% range 0-3 MIPS; 5% range 3-10 MIPS*
Gain	*Adjustable (4 values)*
Sampling frequency	*1MHz to 50MHz*
Shaping Time	*100ns to 2μs*
Read out frequency	*20 to 25MHz*
Polarity of detector signal	*Negative (TPC) or positive*
Calibration	*Selection 1/72*
Test	*one internal test capacitor per channel*

Table 1: List of the requirements

2 Architecture of the analog channel

The architecture of the analog channel has been defined to meet the requirements and specifically to obtain the signal to noise ratio asked and the optimal shaping time for the signal digitalization in the SCA. However, it takes into account the aspects of the consumption power and silicon area. It can also fit all different configurations of detector, as the gain, capacitor and drift velocity, and support the both polarity of the detector signal (positive or negative).

2.1 General description

The analog channel (Fig.3) is composed of four stages:

- C.S.A : Charge Sensitive Amplifier
- PZC: the pole-zero cancellation stage
- R.C^2 filter : Sallen&Key filter
- Gain-2

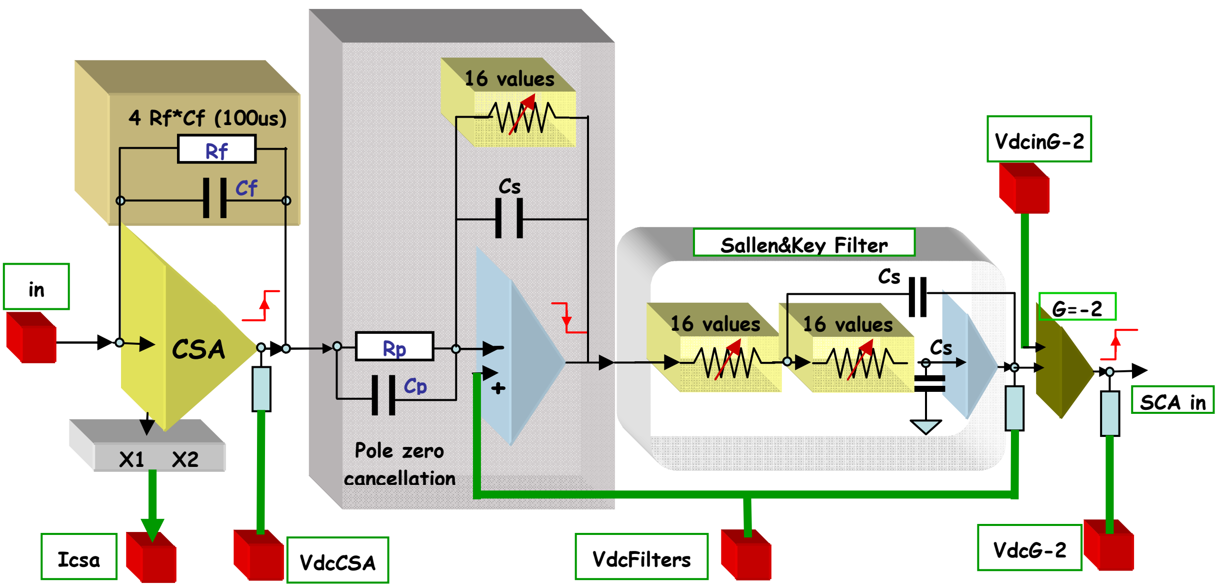


Fig.3: schematic of the analog channel

2.1.A The Charge Sensitive Amplifier

This amplifier is based on single-ended folded cascode architecture. The input transistor is a NMOS device and the dimensions are: 2000µm/0.35µm. The drain current is defined and controlled on ***FEC*** through the pad **126** or **155**. By Slow Control, it's possible to increase or not this current by a factor 2. The value will be fixed (1mA of maximum value) by taking into account the compromise between the noise and the power.

The d.c output voltage is defined also in external through the pad **133** or **148**. A fixed level of 2V allows the CSA to work with the both polarity of the input signal. The linear range of the CSA output voltage is **+/- 600mV**.

The charge to voltage conversion is made by selecting (by Slow Control) one of the four feedback capacitors. The values are: **200fF**, **400fF**, **600f**F and **1pF**.

The feedback resistor is defined by an attenuating current conveyor. We have in fact 4 resistors, each associated with one of the feedback capacitor to obtain a fixed time constant value of 100µs. This value is small enough to avoid any saturation effect of the CSA output even and large compared with the peaking time of the filter (2µs maximum).

2.1.B The pole-zero cancellation stage (PZC)

The PZC stage is used to avoid long duration undershoots at the output. It introduces a pole to cancel the low frequency zero of the CSA and replaces it by a higher tuneable zero. We use the attenuating current conveyor of the CSA to realize the resistor of the pole. A capacitor of 6pF defines the frequency of this pole. The new zero is defined by the couple Rs & Cs, while the value is selected, by Slow Control, between sixteen possible values (50ns to 1µs). The d.c output voltage is defined in external through the pad **134** or **147** and must be adapted to the polarity of the input signal. For the TPC, this reference voltage (2.2V) is set closer to the positive rail so that its output swings towards the negative rail. In the opposite configuration, the voltage must be tied to 0.7V.

2.1.C The R.C^2 filter

With the previous CR filter, this 2-pole Sallen-Key low pass filter gives the total CR-RC^2 semi-Gaussian shaping of the analog channel. The peaking time of the global filter (**CR-RC^2**) is defined by switching different combination of the resistors on each stage, in the same way. The available range is **100ns** to **2µs** (**sixteen values**). The d.c output voltage is defined as the PZC (pin **134** or **147**), and must be adapted to the polarity of the input signal. For the TPC, this reference voltage (2.2V) is set closer to the positive rail so that its output swings towards the negative rail. In the opposite configuration, the voltage must be tied to 0.7V.

2.1.D The Gain-2

This stage provides the voltage dynamic of the chain and the necessary buffering for the sampling of the signal in the SCA. The total dynamic (full range) is 1.5V, limited by the linearity of the SCA. As it is an inverter stage, the dc output level voltage must be set closer to the negative rail to support the positive swing of the signal (0.7V for T2K). This voltage is defined through the pad **135** or **146**. The input common mode voltage is defined by the pads **138** or **142**. These 2 pins are used also to supply the reference voltage of the SCA at a fixed value of 0.7V.

2.2 The Fixed Pattern Noise Channel (F.P.N)

To perform common mode rejection, 4 extra channels FPN (Fixed Pattern Noise) are included in the chip. These channels (Fig.4) are only constituted by the stage Gain-2 which the inputs are connected to the input reference voltage. The F.P.N channels will be treated by the SCA exactly as the other channels. By off-line, their outputs will be subtracted to the 72 analog channels. This pseudo differential operation is supposed to reject the major part of the coherent noise generated before and inside the chip such as clock feed through and couplings through the substrate. It also improves the power supplies rejection ratio (PSRR) of the chip. They are placed uniformly in the chip. Their reading numbers are: 13, 26, 51 & 64.

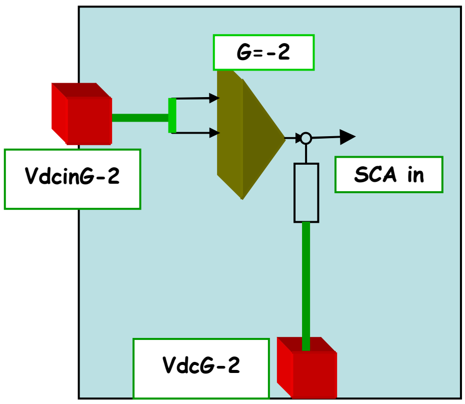


Fig.4: schematic of the FPN analog channel

3 Architecture of the SCA

The analog memory is based on the **S**witched **C**apacitor **A**rray structure. It is used as a circular buffer in which the analog signal coming out from the analog channel is continuously sampled and stored at a sampling rate **Fs**. The sampler is stopped when the ***FEM*** received the external **TRIGGER** signal. Then for each channel, all the 511 samples are read back, starting by the oldest sample. The analog data coming from the 76 channels are time-domain multiplexed and read toward a single external 12_bit ADC channel.

3.1 General description

The Switch Capacitor Array includes 76 channels of each 511 capacitor cells. The cells of a channel are arranged in line and share the same analog bus and a read amplifier. All the cells of the 76 channels (namely a column) are sharing the same write and read column signals. It means that all the cells of a column are written or read at the same time. The write and read operations are performed successively.

3.1.A The memory cell

The memory cell is based on a capacitor of 300fF with 4 switches (Fig.5).

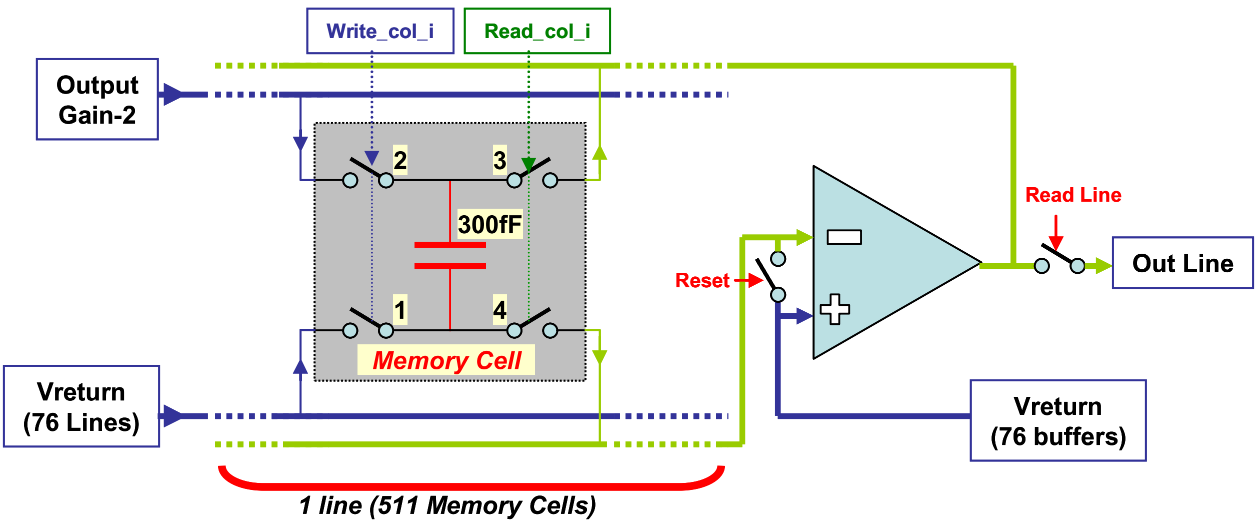


Fig.5: schematic of 1 Memory Cells Line

The Write operation in the cell of column **i** is performed by successively closing and opening the switches 1 and 2 of a cell by the command line ***Write_col_i*** (called the write pointer). The write pointers are the successive outputs of a circular shift register clocked by ***Wck***.

The Read operation in the cell of column **i**, is performed by:

- Resetting the read amplifier and the read bus.
- Closing switches 3 and 4 of a cell by the command line ***Read_col_i*** (called the read pointer).
- Multiplexing the output by an individual command line ***Read_line*** to the chip output.

3.1.B The Readout architecture

To cope with the high read-out frequency **F*rck (20 MHz)***, the 76 channels are divided in two groups: Group 0 for odd number channels (1, 3, … 71) + 2 FPN channels, and Group 1 for even number channels (2, 4, … 72) + 2 FPN channels.

The output multiplexing of the global memory is performed in two stages (Fig.6).

The first channels of the group 0 and group 1 are read and multiplexed each in a first stage at a rate of **F*rck*/2**. The commands of the group 1 are shifted by ***1/Frck*** compared with the group 0. Then the outputs of the second stage are multiplexed at ***1/Frck*** rate to a common buffer. This buffer is necessary for driving the input of the differential output buffer.

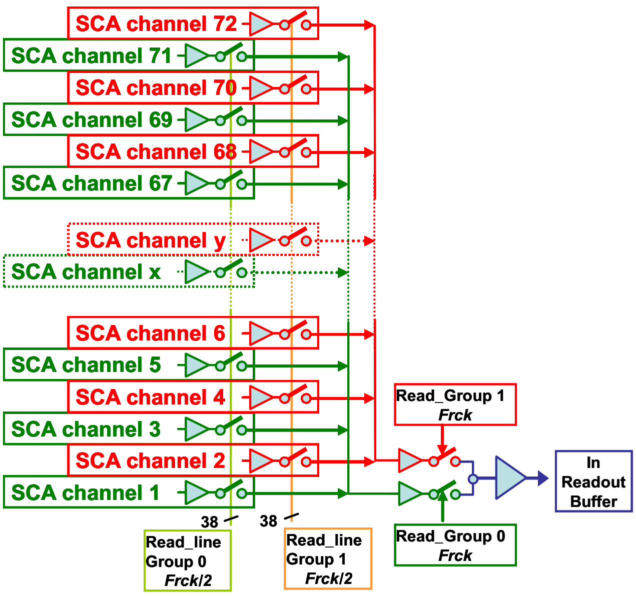


Fig.6: the SCA readout architecture

3.2 Description of the Write and Read phases

The SCA uses 4 digital command signals.

- Two clocks sequencing the write and read operations:
  - Wck : the write clock
  - Rck : the read clock.

These clocks are active on their rising edges, and may be stopped when they are not used.

- Two “envelope” signals defining the write and read operations (Fig.7):
  - Write: defining the write operation.
  - Read: defining the read operation.

These signals are active on their high levels.

The clock signals are provided using differential LVDS levels. The write and read signals are received in CMOS levels.

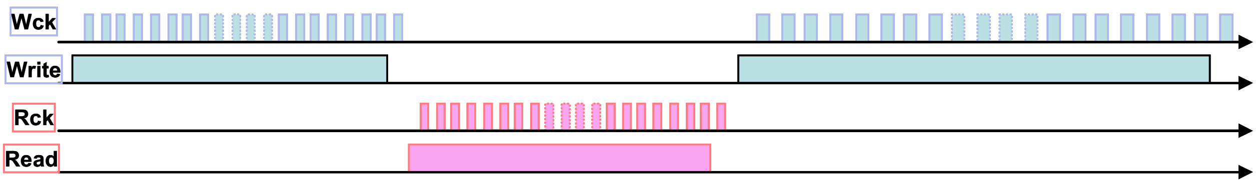


Fig.7: Definition of the write and read phases

3.2.A The Write phase

The write operation is initiated when the ***Write*** signal is set to 1. Its positive edge asynchronously resets the write pointer to the column 0. This pointer is then shifted to the successive columns on the rising edge of ***Wck***, performing the writing operation. When ***Write*** comes back to 0, the write pointer position is frozen and the writing operation is stopped.

The ***Write*** signal can be set or reset on the negative transition of ***Wck.*** Only one ***Wck*** positive edge is needed after the ***Write*** signal falling edge.

3.2.B The Read phase

The read operation is initiated when the ***Read*** signal is set to 1.

Its positive edge asynchronously copies the write pointer to the read pointer and reset the multiplexer register. As long as ***Read*** stays to 1, the analog signals are sequentially multiplexed to the output at each rising edge of the ***Rck***. The first column read is the one following the last written. To read a column, 78 ***Rck*** periods are needed (Fig.8). The two firsts are corresponding to reset level of read-amplifiers, the 76 following are corresponding to the analog data stored in the different lines of the column starting from line 1 and multiplexed alternately from group 0 and group 1. After the last (76^{th}) cell of this column, the read pointer is shifted and the same operation is performed on the next column.

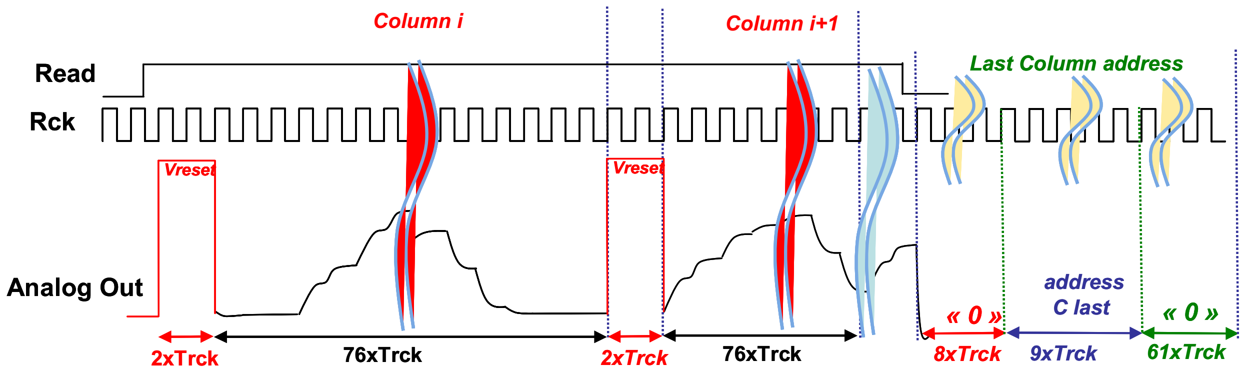


Fig.8: Read phase

When ***Read*** comes back to 0, this sequence is asynchronously interrupted and the current address of the read pointer is encoded and multiplexed to the output. The negative ***Read*** transition can occur whenever the controller decides it. This allows reading a limited number of cells. Eight 0 are first sent to the output, then the 9-bit address of the read address (MSb first), then sixty-one more 0 (to be compatible with the 78 samples format of a column). This operation is then terminated or it can be also stopped if ***Write*** is set to 1.

After this, the output comes back to the reset level of the line 1 read amplifier.

As for Write, it could be convenient to set or reset the ***Read*** signal on the negative edge of ***Rck***.

The read sequence of the 76 channels is summarized in the table 2.

Data out bit	Channel Number	Pin Number	Data out bit	Channel Number	Pin Number
1	1	36	39	37	120
2	2	35	40	38	119
3	3	34	41	39	118
4	4	33	42	40	117
5	5	32	43	41	116
6	6	31	44	42	115
7	7	30	45	43	114
8	8	29	46	44	113
9	9	28	47	45	112
10	10	27	48	46	111
11	11	26	49	47	110
12	12	25	50	48	109
13	FPN1		51	FPN3	
14	13	24	52	49	108
15	14	23	53	50	107
16	15	22	54	51	106
17	16	21	55	52	105
18	17	20	56	53	104
19	18	19	57	54	103
20	19	18	58	55	102
21	20	17	59	56	101
22	21	16	60	57	100
23	22	15	61	58	99
24	23	14	62	59	98
25	24	13	63	60	97
26	FPN2		64	FPN4	
27	25	12	65	61	96
28	26	11	66	62	95
29	27	10	67	63	94
30	28	9	68	64	93
31	29	8	69	65	92
32	30	7	70	66	91
33	31	6	71	67	90
34	32	5	72	68	89
35	33	4	73	69	88
36	34	3	74	70	87
37	35	2	75	71	86
38	36	1	76	72	85

Table 2: Description of data readout frame

4. Architecture of the Readout Buffer

This buffer must drive the external 12_bits ADC (AD9229) at 20 MHz of readout frequency. It is a single ended input to differential output with a gain of 1.33 to fit the input dynamic of the ADC (+/- 1V on each input).

The buffer must support the ADC input architecture and take into account the effects of the interconnection on the ***FEC*** (parasitic capacitors & coupling). The main constraint concerns the settling time of the signal, for which the error must be less than 1/1000 of the total dynamic range (settling time < $T_{CKread}/2$ = 25ns).

This buffer (Fig.9) has two feedback loops. One controls the common mode output voltage. Its input is ***vocm*** (Pin 68) and the output is the common-mode, or average voltage, of the two differential outputs ***vop*** (pin 73) and ***von*** (pin 74). The gain of this circuit is internally set to unity. The level must be set to ***VddADC/2*** (1.65V).

The second feedback loop controls the differential operation. The gain, made by the ratio of two resistors, is equal to 1.33.

The positive input is connected to the output buffer of the SCA. The negative input is supplied through a pad (pin 71) at a level corresponding to:

[Vdc*GAIN-2* +/- Vmax*OutputSignalGAIN-2*]/2

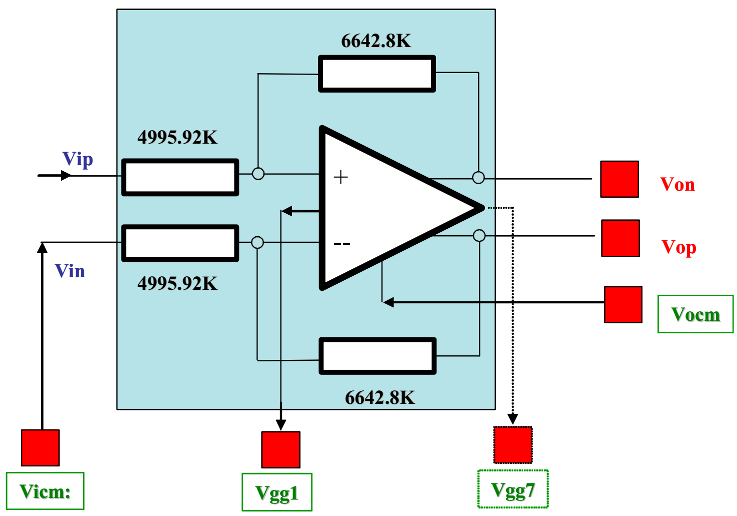


Fig.9: schematic of the readout buffer

5. Architecture of the Test system & "spy" mode

An important implemented feature concerns the test system which will be used for: electrical calibration, asic test bench and functionality control of all electronic channels (Asic to acquisition board). We have also the possibility to view on scope 3 important signals of the analog channel number 1: CSA, CR and Gain-2 outputs.

5.1 General description of the test system

The asic AFTER has 3 different modes of test: calibration, test and functionality. Calibration implies to generate a same charge on all channels of all asics on the same FEC or all FEC of a TPC plan. Therefore, the charge generation is made outside of the chip, directly on the FEC. The principal components are 12 bits DAC, a buffer amplifier and capacitor. The charge generation is made by applying a small voltage step to a capacitor at the input of the channel selected. The selection is made inside the chip by slow control (Fig.10).

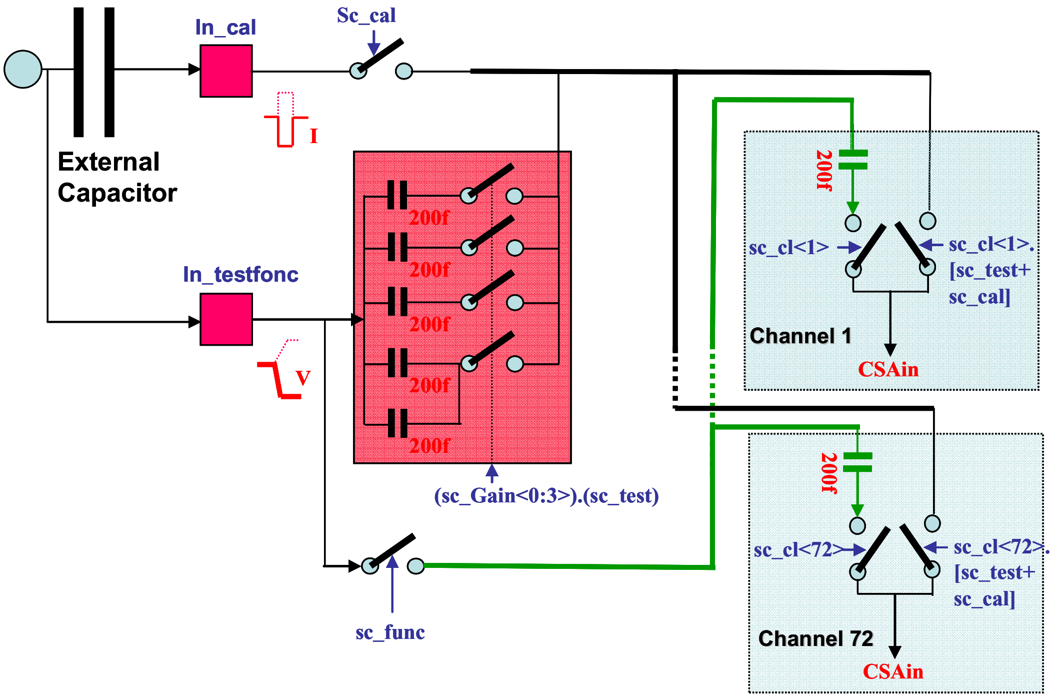


Fig.10: schematic of the test system

The current charge is delivering on the pad ***In_cal*** (pin 39). For the 2 other modes, only the pulse generator is used. The current charge is made through internal capacitors. The voltage step is received on the pad ***In_testfonc*** (pin 40). For the test, we have four injection capacitors, one for each energy range. This provides to work with the same dynamic level of pulse generator. The selection of the capacitor is automatically done when the energy range is selected.

For the functionality, we have one capacitor (200fF) per channel. For the 3 modes, the selection of the channel must be made by slow control. For the third mode, all the 76 channels can be selected.

For the FPN channel, only the functionality test can be used. The input voltage step is applied directly to the input of the GAIN-2 stage of the selected FPN channel.

5.2 General description of the “spy” mode

This mode gives the possibility to view directly on a scope the outputs of the CSA, CR filter and Gain-2 from the channel number 1. This feature will be useful to understand the source and the reason of any mismatch between experimental and theoretical results. By slow control, one of these 3 signals (Fig.11) is switched, through an internal buffer, to the pad ***Out_debug*** (pin 46). If the “spy” mode is not selected, the internal buffers are put in a standby mode.

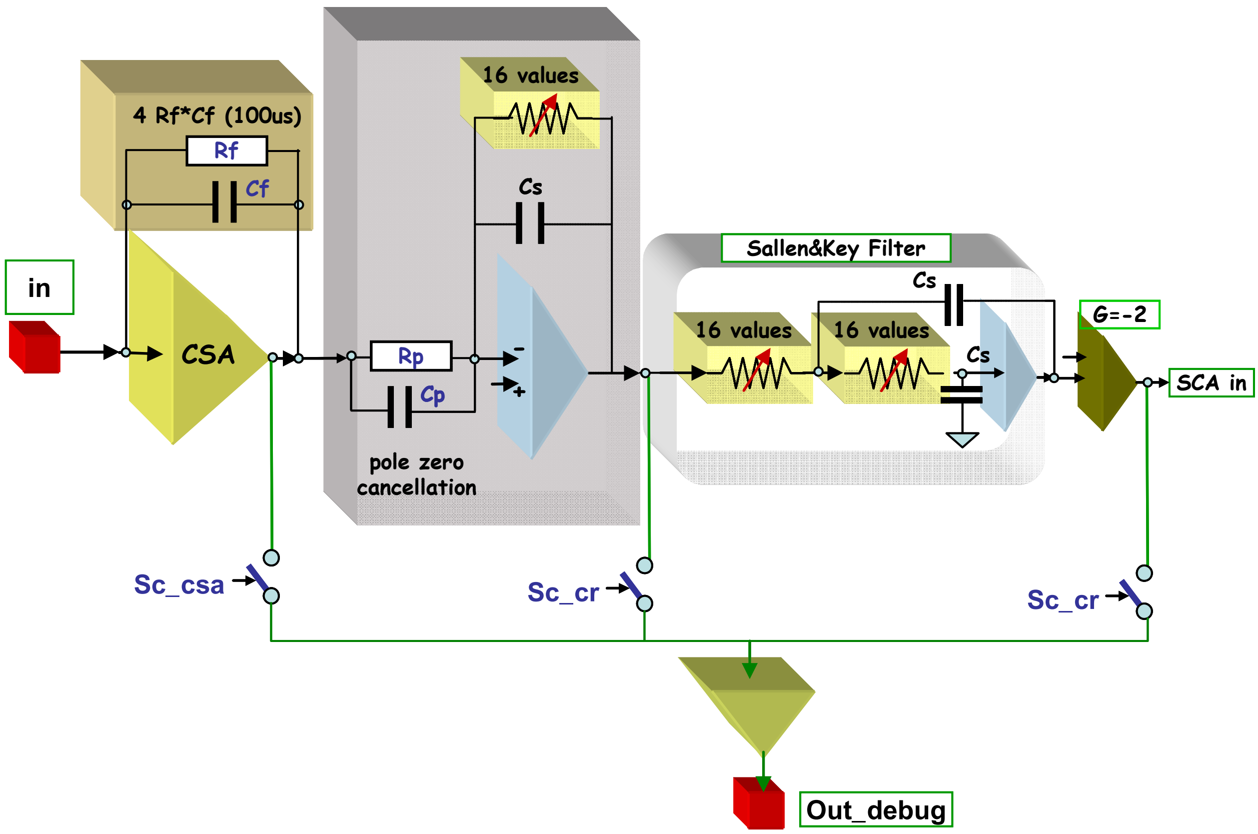


Fig.11: schematic of the “spy” mode

6. The Slow Control

The slow control provides to select the different modes of functionality (gain, shaping time, test mode …). It is a serial protocol, used in several ASICs of SACLAY laboratory. It gives access in write or read mode to the four internal registers which their address are coded in 7 bits. The depth of the 2 configuration registers is 16 bits, and 38 bits for the two others dedicated for the channel selection to be tested.

6.1 Init phase

With the powering, an internal device delivers a reset pulse (about 1ms of duration) to the 4 registers.

6.2 Description of the serial link.

The link uses **4** signals of level **CMOS** [0V; 3.3V]:

- ***Sc_din [pin N°51]***: input data of the serial link.
- ***Sc_ck [pin N°53]***: clock of the serial link.
- ***Sc_en [pin N°52]***: enable of the serial link.
- ***Sc_dout [pin N° 54]***: output data of the serial link.

The signals ***Sc_din*** & ***Sc_en*** must be synchronous to the rising edge of ***Sc_ck.*** The data are sampled on the input lines, decoded and operations of reading/writing are carried out on the falling edge of ***Sc_ck***. Thus, the data at the output of ***Sc_dout*** will be synchronous on this edge.

On ***Sc_din,*** the data packet is defined as:

[**r/wb**] [**Ad6… Ad0**] [**DNBD-1…D0**]

[**r/wb**]: This first bit defines the type of operation. **r/wb** =1 : readout; 0: write.

[**Ad6… Ad0**]: These 7 bits give the address of the target register.

[**DNBD-1…D0**]: This is the **NBD** bits of the data.

The most significant bit of the address and the data is always sending (or reading) in first.

The ***Sc_en*** signal frames the data sent on ***Sc_din***. It must go up simultaneously with the positioning of [**r/wb**] and must go down one cycle of ***Sc_ck*** after the positioning of the last bit of data (***D0***) on ***Sc_din***. Thus, the data packet defined by the setting of the ***Sc_en*** signal to 1 must frame [***8+ NBD*** falling edges**]** of ***Sc_ck***.

The ***Sc_ck*** clock must be present immediately after the beginning of the data packet and must continue at least during three clocks (falling edge) after the falling edge of ***Sc_en***.

The ***Sc_dout*** keeps the last enable level. Outside the data packet, the level of ***Sc_ck*** can be "0" or "1".

6.3 Resynchronisation on Sc_dout.

All the data on the *Sc_dout* line are, by default, locally synchronised on the *Sc_ck* falling edge. But this synchronising is partially lost due to the different transit times in the chip. It is also possible, by slow control, to synchronise the signal on ***Sc_dout***. This is done by the bit 9 (***out_resync***) of the register 2, and the choice of active edge by the bit 10 (***synchro_inv***). If the state is "1", the synchronisation will be made on the falling edge of ***Sc_ck***; "0" on the rising edge. All the chronograms on the next figures are in the case where the bit ***out_resync*** is "0".

6.4 Writing mode (address other that 0) in a register of C bits.

The write mode (Fig.12) is defined by the first bit **r/wb = 0**. The falling edge of ***Sc_en*** starts the writing of the **C** last bits on ***Sc_din*** in the target register. After the eighth falling edge of ***Sc_ck***, ***Sc_dout*** leaves its quiet level. During **C** clocks, ***Sc_dout*** takes the **Y<n :1>** states, according to the history on the **Sc_din** line. Then, it will take the states present **C** clocks before (A<0>, D<15>, D<14> in the normal case where C=NBD).

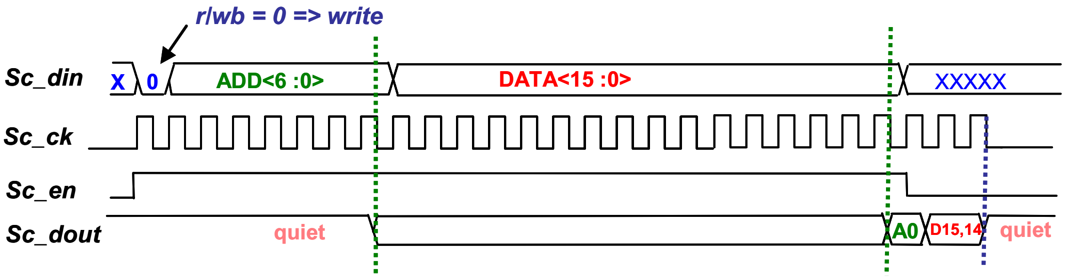


Fig.12: Write phase

Sc_dout will take the quiet level 3 rising edges of the clock after the falling of ***Sc_en***.

The number of **NBD** bits present in the data part of ***Sc_din*** can be greater than the size of the register (**C** bits). In this case, only the **C** last bits will be written in the register. The **NBD-C-2** first bits of the data will go out on the ***Sc_dout*** after A0, D15 & D14. This feature can be used to test the serial link.

6.5 Register 0 case.

The register **0** doesn't exist physically. But, when it is addressed in write mode, ***Sc_dout*** recopy the data on ***Sc_din*** (after the eighth falling edge of ***Sc_ck***). ***Sc_dout*** go back to the quiet state (3 rising edges after the falling edge of ***Sc_en***).

6.6 Reading phase of a C bits Register.

In the readout mode (Fig.13), ***Sc_en*** must cover more than **8+C-2** falling edges of ***Sc_ck***. A minimum of 3 falling edges of ***Sc_ck*** after the falling of ***Sc_en***, is necessary to finish the reading phase.

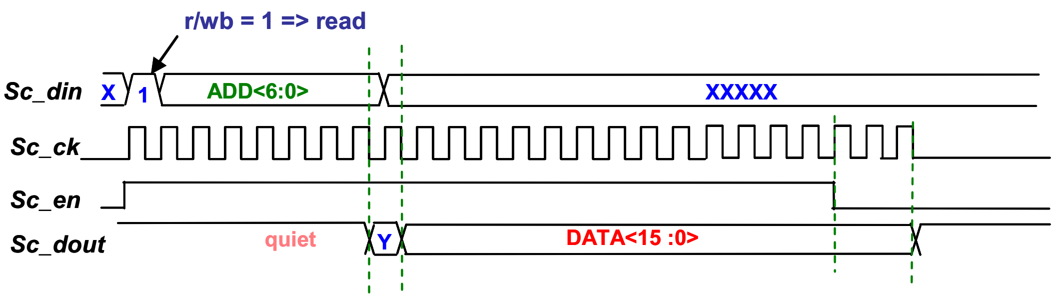


Fig.13: Read phase

The first bit on ***Sc_din*** must be to "1" (**r/wb**)**.** Thus the 7 other bits define the address of the register. The next bits can be indefinite.

At the eighth falling edge of ***Sc_ck***, the address is decoded and ***Sc_dout*** leaves its quiet level. During 1 clock cycle, its state **Y** depends on history of the serial link.

At the ninth falling edge of ***Sc_ck***, the data of the register go to the ***Sc_dout*** during **C** clock cycles. After **C** clock cycles, the data on the ***Sc_dout*** are not valid.
As for the writing phase, ***Sc_dout*** go back to its quiet level, **3** clock cycles after the falling edge of ***Sc_en***.

6.7 Description of the registers

The chip AFTER has 4 registers; 2 of 16 bits and 2 of 38 bits.

6.7.1 Register 1

This register of 16 bits has the address number 1 (table 3). The 9 first bits define the configuration for the analog part of the channel before the SCA. The last 3 bits provide to control the power consumption of the chip.

bit	name	action
0	**Icsa**	if 1, the nominal CSA bias current is x2
1	**Gain0**	LSB of the gain tuning
2	**Gain1**	MSB of the gain tuning
3	**Time0**	LSB of the filter peaking time
4	**Time1**	bit 1 of the filter peaking time
5	**Time2**	bit 2 of the filter peaking time
6	**Time3**	MSB of the filter peaking time
7	**Test0**	LSB of the test mode register
8	**Test1**	MSB of the test mode register
9		
10		
11		
12		
13	**power_down_write**	if 1, put the write section in power down mode
14	**power_down_read**	if 1put the read section in power down mode
15	**alternate_power**	if 1, set alternatively the read and write sections in power down mode.

Table 3: Description of the register 1

- ***bit Gain0 to Gain1:***

These 2 bits define the input energy range. This range is made by selecting one feedback capacitor between 4 on the C.S.A (table 4).

Gain1	Gain0	Energy Range
0	**0**	***120fC***
0	**1**	***240fC***
1	**0**	***360fC***
1	**1**	***600fC***

Table 4: Definition of the dynamic range

* ***bit Time0 to Time3:***

These 4 bits fixe the peaking time of the shaping (table 5), by switching resistors on the CR & SK filters.

Time3	Time2	Time1	Time0	Peaking Time
0	0	0	0	*100ns*
0	0	0	1	*200ns*
0	0	1	0	*400ns*
0	0	1	1	*500ns*
0	1	0	0	*600ns*
0	1	0	1	*700ns*
0	1	1	0	*900ns*
0	1	1	1	*1000ns*
1	0	0	0	*1100ns*
1	0	0	1	*1200ns*
1	0	1	0	*1400ns*
1	0	1	1	*1500ns*
1	1	0	0	*1600ns*
1	1	0	1	*1700ns*
1	1	1	0	*1900ns*
1	1	1	1	*2000ns*

Table 5: Definition of the peaking time

* ***bit Test0 to Test1:***

These bits define the test mode (table 6).

Test1	Test0	Test mode
0	0	*nothing*
0	1	*calibration*
1	0	*test*
1	1	*functionality*

Table 6: Definition of the test mode

Calibration, test & functionality imply to choose one or several channels. This choice is done by the registers 3 & 4.

* ***bits* power_down_write, power_down_read & alternate_power.**

These bits give the possibility to manage the power consumption by the fact that when the chip is in the write mode, the reading part is not used and therefore the SCA line buffer can be put in a standby mode. In the read mode, as the analog data is stored in the SCA, the writing part of the analog channel (pole-zero cancellation stage, Sallen&Key filter and Gain-2) can be put also in a standby mode. This functional mode is activated by the bit ***alternate_power***. It is also possible to force independently the writing and the reading parts in a standby mode by the bits ***power_down_write*** and ***power_down_read***. The effects of this mode on the power consumption are presented in the paragraph 9.1 (page 36).

6.7.2 Register 2

This 16 bits register has the address n°2. It will be used for the test and the control of the SCA reading (table 7).

bit	name	action
0	**debug0**	LSB of the debug mode register
1	**debug1**	MSB of the debug mode register
2		
3	**read_from_0**	if 1, force to start the readout from column 0
4	**test_digout**	if 1, a test pattern is serialized to the output instead of the 9bit address of the last read column
5	**set_l0_when_rst**	if 1, the d.c output voltage of the Gain-2 (Vdc_g2d) is multiplexed to the analog output during "reset operation"
6	**en_mker_rst**	if 1, a "digital" marker (near gnd or vdd levels) is multiplexed to the analog output during "reset operation"
7	**rst_lv_to 1**	set the level of the digital marker (when en_mker_rst=1)
8	**boost_pw**	If 1, the output current of the analog block Gain-2 is increased (+20%)
9	**out_resync**	If 1, the SC output data is resynchronized by a clock edge (selected by synchro_inv)
10	**synchro_inv**	select the edge for the synchronizing of the SC output data (0= rising, 1=falling)
11	**force_eout**	If 1, inhibit the 3rd state functionality of the SC output buffer.
12	**Cur_RA<0>**	These 2 bits manage the current of the SCA line buffers
13	**Cur_RA<1>**	
14	**Cur_BUF<0>**	These 2 bits manage the current of the SCA output buffers
15	**Cur_BUF<1>**	

Table 7: Description of the register 2

- ***bit Debug0 to Debug1***

These 2 bits allow us to view on a scope the outputs of the CSA, CR filter and Gain-2 from the channel number 1. One of these outputs (table 8) will be switched to the pad ***Out_debug*** [pin N° 46].

Debug1	Debug0	Out_debug (canal1)
0	**0**	***Standby***
0	**1**	***CSA***
1	**0**	***CR***
1	**1**	***Gain2***

Table 8: Selection of the output in the "spy" mode

- **read_from_0; test_digout; set_I0_when_rst; en_mker_rst; rst_lv_to 1.**

These 5 bits act directly on the readout of the SCA and will be used essentially for the test of the asic and FEC prototypes.

read_from_0: In the normal mode, the readout starts from the column following the last written. Put this bit to “1”, force to start the readout from the column **0**.
test_digout: if “1”, a test pattern (“10101100”) is serialized to the output instead of the 9bit address of the last read column.
set_I0_when_rst: if “1”, the d.c output voltage of the Gain-2 (Vdc_g2d) is multiplexed to the analog output during "reset operation".
en_mker_rst: If “1”, a "digital" marker (near gnd or vdd levels) is multiplexed to the analog output during "reset operation".
rst_lv_to 1: Set the level of the digital marker (when en_mker_rst=”1”). “0” means level near gnd; “1” means level near Vdd.

- ***bit*** **boost_pw.**

If 1, the output current of the analog block GAIN-2 is increased by +20%. It gives the possibility to compensate a value much smaller due to the variations of the process parameters, in the case where the write frequency will be around 50MHz.

- ***bit*** **out_resync, synchro_inv & force_eout**

These 3 bits change some configurations for the Slow Control.

out_resync: If 1, the ***Sc_dout*** output data is resynchronized by a clock edge ***Sc_ck***, selected by ***synchro_inv***.
synchro_inv: Selects the edge for the synchronizing of the ***Sc_dout*** output data. “0” select the rising edge, “1” the falling.
force_eout: “1” inhibits the 3rd state functionality of the SC output buffer.

- ***bits*** **CUR_RA <1:0>**

These 2 bits control the current of the 76 SCA line readout buffers. This control is also managed by the bits ***power_down_read*** & ***alternate_power*** of the register 1. The table 9 gives the different values.

		power_down_read & ***alternate_power = "0"***	***power_down_read*** or ***alternate_power = "1"***
CUR_RA<1>	**CUR_RA<0>**	**I power**	**I power**
0	**0**	***211uA***	***172uA***
0	**1**	***274uA***	***211uA***
1	**0**	***395uA***	***274uA***
1	**1**	***735uA***	***395uA***

Table 9: Control of the SCA line buffer current

The nominal configuration is: « **10** ».

- ***bits*** **CUR_BUF <1:0>**

These 2 bits control the current of the SCA readout buffer of the 2 groups (one buffer for 38 lines) and also the SCA readout buffer (Fig.6). The tables 10&11 show the different values for the 2 buffers.

CUR_BUF<1>	**CUR_BUF<0>**	**I power on SCA group buffer**
0	**0**	***132uA***
0	**1**	***169uA***
1	**0**	***239uA***
1	**1**	***433uA***

Table 10: Control of the SCA group buffer current

CUR_BUF<1>	**CUR_BUF<0>**	**I power on SCA output buffer**
0	**0**	***482uA***
0	**1**	***620uA***
1	**0**	***831uA***
1	**1**	***1.610mA***

Table 11: Control of the SCA output buffer current

The nominal configuration is: « **10** ».

6.7.3 Register 3

This 38 bits register has the address number 3. It is used to select the channel for the test (table 12). The channel number goes from 1 to 36, and 1 to 2 for the FPN channel.

bit	name	action
0	**select_c36**	Selection of the channel 36 for the test
1	**select_c35**	Selection of the channel 35 for the test
2	**select_c34**	Selection of the channel 34 for the test
3	**select_c33**	Selection of the channel 33 for the test
4	**select_c32**	Selection of the channel 32 for the test
5	**select_c31**	Selection of the channel 31 for the test
6	**select_c30**	Selection of the channel 30 for the test
7	**select_c29**	Selection of the channel 29 for the test
8	**select_c28**	Selection of the channel 28 for the test
9	**select_c27**	Selection of the channel 27 for the test
10	**select_c26**	Selection of the channel 26 for the test
11	**select_c25**	Selection of the channel 25 for the test
12	**select_cfpn2**	Selection of the channel cfpn2 for the test
13	**select_c24**	Selection of the channel 24 for the test
14	**select_c23**	Selection of the channel 23 for the test
15	**select_c22**	Selection of the channel 22 for the test
16	**select_c21**	Selection of the channel 21 for the test
17	**select_c20**	Selection of the channel 20 for the test
18	**select_c19**	Selection of the channel 19 for the test
19	**select_c18**	Selection of the channel 18 for the test
20	**select_c17**	Selection of the channel 17 for the test
21	**select_c16**	Selection of the channel 16 for the test
22	**select_c15**	Selection of the channel 15 for the test
23	**select_c14**	Selection of the channel 14 for the test
24	**select_c13**	Selection of the channel 13 for the test
25	**select_cfpn1**	Selection of the channel cfpn1 for the test
26	**select_c12**	Selection of the channel 12 for the test
27	**select_c11**	Selection of the channel 11 for the test
28	**select_c10**	Selection of the channel 10 for the test
29	**select_c9**	Selection of the channel 9 for the test
30	**select_c8**	Selection of the channel 8 for the test
31	**select_c7**	Selection of the channel 7 for the test
32	**select_c6**	Selection of the channel 6 for the test
33	**select_c5**	Selection of the channel 5 for the test
34	**select_c4**	Selection of the channel 4 for the test
35	**select_c3**	Selection of the channel 3 for the test
36	**select_c2**	Selection of the channel 2 for the test
37	**select_c1**	Selection of the channel 1 for the test

Table 12: Description of the register 3

6.7.4 Registre 4

This 38 bits register has the address number 4. It is used to select the channel for the test (table 13). The channel number goes from 37 to 72, and 3 to 4 for the FPN channel.

bit	name	action
0	**select_c37**	Selection of the channel 37 for the test
1	**select_c38**	Selection of the channel 38 for the test
2	**select_c39**	Selection of the channel 39 for the test
3	**select_c40**	Selection of the channel 40 for the test
4	**select_c41**	Selection of the channel 41 for the test
5	**select_c42**	Selection of the channel 42 for the test
6	**select_c43**	Selection of the channel 43 for the test
7	**select_c44**	Selection of the channel 44 for the test
8	**select_c45**	Selection of the channel 45 for the test
9	**select_c46**	Selection of the channel 46 for the test
10	**select_c47**	Selection of the channel 47 for the test
11	**select_c48**	Selection of the channel 48 for the test
12	**select_cfpn3**	Selection of the channel cfpn3 for the test
13	**select_c49**	Selection of the channel 49 for the test
14	**select_c50**	Selection of the channel 50 for the test
15	**select_c51**	Selection of the channel 51 for the test
16	**select_c52**	Selection of the channel 52 for the test
17	**select_c53**	Selection of the channel 53 for the test
18	**select_c54**	Selection of the channel 54 for the test
19	**select_c55**	Selection of the channel 55 for the test
20	**select_c56**	Selection of the channel 56 for the test
21	**select_c57**	Selection of the channel 57 for the test
22	**select_c58**	Selection of the channel 58 for the test
23	**select_c59**	Selection of the channel 59 for the test
24	**select_c60**	Selection of the channel 60 for the test
25	**select_cfpn4**	Selection of the channel cfpn4 for the test
26	**select_c61**	Selection of the channel 61 for the test
27	**select_c62**	Selection of the channel 62 for the test
28	**select_c63**	Selection of the channel 63 for the test
29	**select_c64**	Selection of the channel 64 for the test
30	**select_c65**	Selection of the channel 65 for the test
31	**select_c66**	Selection of the channel 66 for the test
32	**select_c67**	Selection of the channel 67 for the test
33	**select_c68**	Selection of the channel 68 for the test
34	**select_c69**	Selection of the channel 69 for the test
35	**select_c70**	Selection of the channel 70 for the test
36	**select_c71**	Selection of the channel 71 for the test
37	**select_c72**	Selection of the channel 72 for the test

Table 13: Description of the register 4

7. The power supply.

The chip AFTER have a significant number of pins (27 VDD + 30 GND) dedicated to the supply. The architecture divides the number of analog channels into 2 groups of 38, for matching a square package. The height of these 2 groups (7mm) and the sensitivity of each block (CSA, CR, SK & G-2) imply to supply these blocks independently and homogeneous (Pins in top and bottom). This is also used for the SCA. The Fig.14 shows the internal architecture of the chip by indicating the placement and the name of the various building blocks.

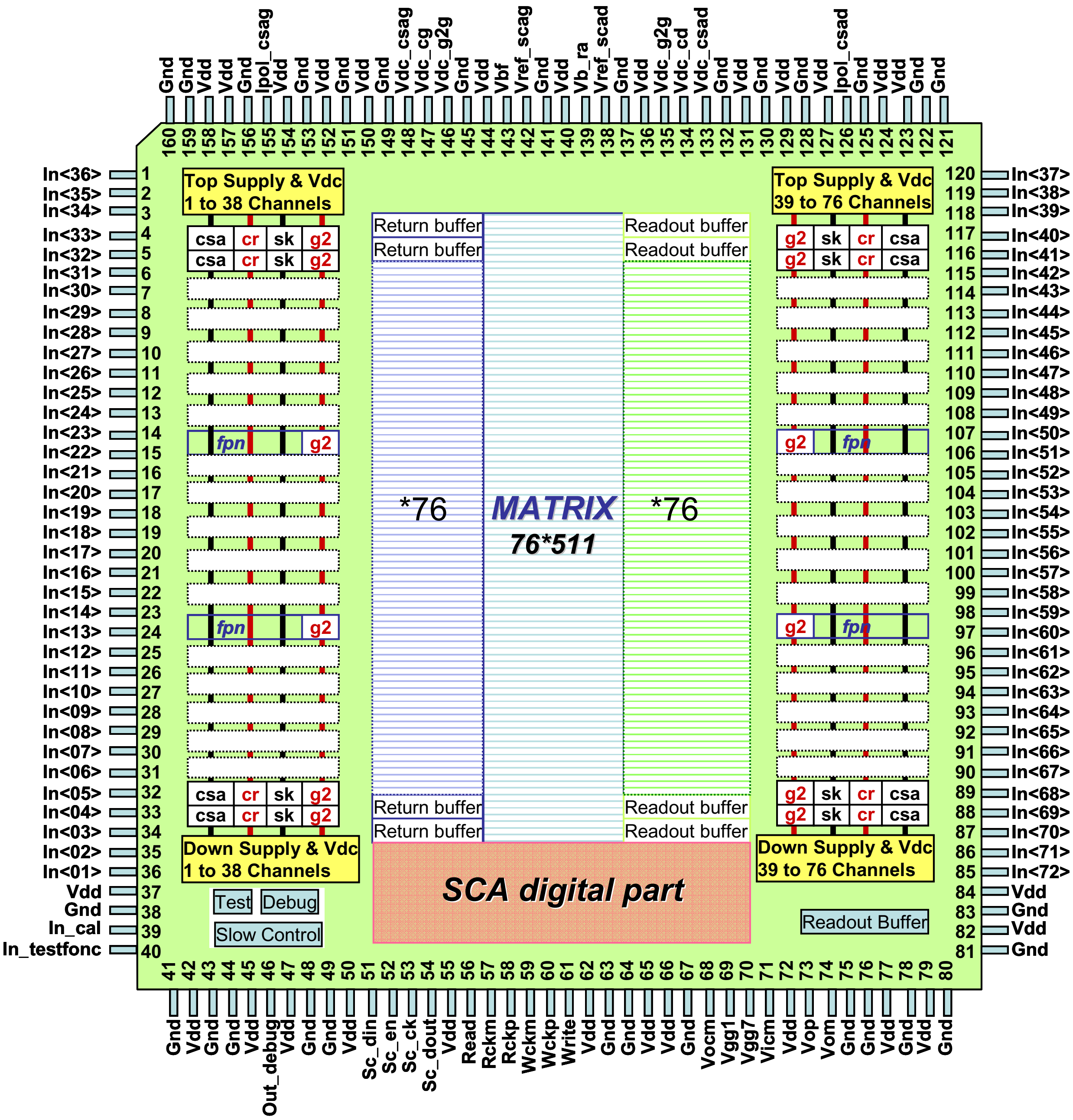


Fig.14: internal architecture of AFTER

7.1 Polarization of the cavity

The substrat (P type) must be polarized to the ground. This is done by polarizing the bottom of the cavity with 4 pins (Fig.15).

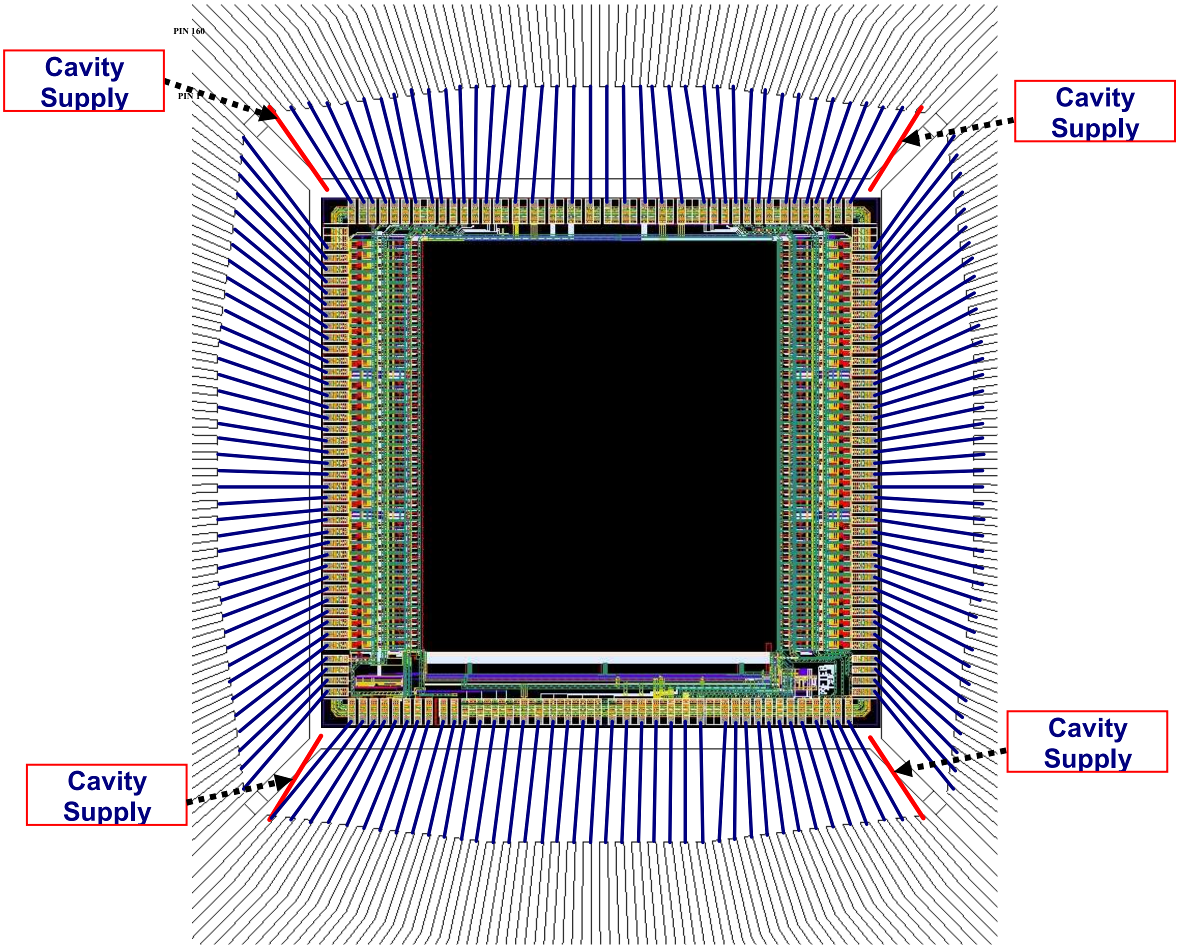


Fig.15: bonding diagram of AFTER

N° Pin	*Name*	*I dc*	*Description*
41	**Gnd_Substrat**	0A	Protection diode [37 to 84],cavity, SCA digital part guard ring & Slow Control
80	**Gnd_Substrat**	0A	Cavity
121	**Gnd_Substrat**	0A	Cavity
160	**Gnd_Substrat**	0A	Cavity

Table 14: Pins for the cavity polarization

The pin 41 is also used for:

- protection diodes of pins 37 to 84,
- guard ring of the digital part of the SCA,
- Slow Control.

7.2 Polarization of the protection diodes

All the pins of the chip have protection diodes. The polarization of these diodes is carried out by independent pins, not used for the polarization of internal blocks (except N° 55).

N° Pin	*Name*	*I dc*	*Description*
55	**Vdd_prob**	0A	Vdd for protection diode [37 to 84], SCA digital part guard ring & Slow Control
41	**Gnd_prob**	0A	Gnd for protection diode [37 to 84], SCA digital part guard ring & Slow Control
123	**Vdd_proind**	0A	Vdd for protection diode [37 to 72]:channels input
122	**Gnd_proind**	0A	Gnd for protection diode [37 to 72]:channels input
140	**Vdd_proh**	0A	Vdd for protection diode 124 to 157]
141	**Gnd_proh**	0A	Gnd for protection diode 124 to 157]
158	**Vdd_proing**	0A	Vdd for protection diode [1 to 36]:channels input
159	**Gnd_proing**	0A	Gnd for protection diode [1 to 36]:channels input

Table 15: Pins for the protection diodes polarization

7.3 Polarization of the analog channels

The analog channel has 4 blocks:

- CSA (table 16),
- CR filter (table 17),
- SK filter (table 18),
- Gain -2 (table 19).

7.3.a) CSA

N° Pin	*Name*	*I dc*	*Description*
37	**Vdd_csag**	2.43mA + Ipol_csag*[1 + 18*(1 or 2)]	**Vdd&Gnd for the CSA of the channel 36 to 1**
38	**Gnd_csag**	2.43mA + Ipol_csag*[1 + 18*(1 or 2)]	
157	**Vdd_csag**	2.43mA + Ipol_csag*[1 + 18*(1 or 2)]	
156	**Gnd_csag**	2.43mA + Ipol_csag*[1 + 18*(1 or 2)]	
84	**Vdd_csad**	2.43mA + Ipol_csad*[1 + 18*(1 or 2)]	**Vdd&Gnd for the CSA of the channel 37 to 72**
83	**Gnd_csad**	2.43mA + Ipol_csad*[1 + 18*(1 or 2)]	
124	**Vdd_csad**	2.43mA + Ipol_csad*[1 + 18*(1 or 2)]	
125	**Gnd_csad**	2.43mA + Ipol_csad*[1 + 18*(1 or 2)]	

Table 16: CSA supply

The d.c current depends of 2 parameters:

- Ipol_csag (N° 155) / Ipol_csad (N° 124) : Nominal current of the CSA, defined on the FEC,
- Factor 1 or 2: given by the 2^0 bit of the register 1 (slow control). If « 0 », factor 1; if « 1 » factor 2.

7.3.b) CR filter

N° Pin	*Name*	*I dc*	*I dc (power down)*	*Description*
42	**Vdd_crg**	3.9mA	1.1mA	**Vdd&Gnd for the CR of the channel 36 to 1**
43	**Gnd_crg**	3.9mA	1.1mA	
154	**Vdd_crg**	3.9mA	1.1mA	
153	**Gnd_crg**	3.9mA	1.1mA	
82	**Vdd_crd**	3.9mA	1.1mA	**Vdd&Gnd for the CR of the channel 37 to 72**
81	**Gnd_crd**	3.9mA	1.1mA	
127	**Vdd_crd**	3.9mA	1.1mA	
128	**Gnd_crd**	3.9mA	1.1mA	

Table 17: CR supply

7.3.c) SK filter

N° Pin	*Name*	*I dc*	*I dc (power down)*	*Description*
45	**Vdd_skg**	1.9mA	740uA	**Vdd&Gnd for the SK of the channel 36 to 1**
44	**Gnd_skg**	1.9mA	740uA	
152	**Vdd_skg**	1.9mA	740uA	
151	**Gnd_skg**	1.9mA	740uA	
79	**Vdd_skd**	1.9mA	740uA	**Vdd&Gnd for the SK of the channel 37 to 72**
78	**Gnd_skd**	1.9mA	740uA	
129	**Vdd_skd**	1.9mA	740uA	
130	**Gnd_skd**	1.9mA	740uA	

Table 18: SK supply

7.3.d) Gain-2

N° Pin	*Name*	*I dc*	*I dc (power down)*	*Description*
47	**Vdd_g2g**	6.881mA	1.73mA	**Vdd&Gnd for the Gain-2 of the channel 36 to 1 + 2 FPN**
48	**Gnd_g2g**	6.881mA	1.73mA	
150	**Vdd_g2g**	6.881mA	1.73mA	
149	**Gnd_g2g**	6.881mA	1.73mA	
77	**Vdd_g2d**	6.881mA	1.73mA	**Vdd&Gnd for the Gain-2 of the channel 37 to 72 + 2FPN**
76	**Gnd_g2d**	6.881mA	1.73mA	
131	**Vdd_g2d**	6.881mA	1.73mA	
132	**Gnd_g2d**	6.881mA	1.73mA	

Table 19: Gain-2 supply

7.4 Polarization of the SCA

For polarization, the SCA is broken up into 4 parts:

- The matrix [511*76 analog cells],
- The input stage "buffer return" [1 per line] (table 20),
- The line buffer stage [1 per line] (table 21),
- The digital part [clock, address …] (table 22).

7.4.a) The matrix

The polarization of the matrix is made by a metal grid on its entire surface. This grid is connected to the bus supply of the « buffer return » and the output. The D.C current is zero.

7.4.b) The input stage « buffer return »

This stage plugs the analog memory capacitance (Fig.5) to a reference, called ***Vreturn***, defined outside by the pad **142** (Vref_scag).

N° Pin	*Name*	*I dc*	*Description*
50	**Vdd**	3.676mA	**Vdd&Gnd for the "buffer return" & Matrix**
49	**Gnd**	3.676mA	
144	**Vdd**	3.676mA	
145	**Gnd**	3.676mA	

Table 20: Supply of the « buffer return »

7.4.c) The SCA line buffer

In the reading phase, this line buffer transmits the data of the memory cells towards the intermediate reading buffer. The current value is adjustable by slow control (page 24).

N° Pin	*Name*	*I dc*	*Description*
66	**Vdd**	6.62mA	**Vdd&Gnd for the SCA readout Amplifier & Matrix (configuration: Cur_RA<1>: "1"; Cur_RA<0>:"0" and Power_down_write: "0")**
67	**Gnd**	6.62mA	
136	**Vdd**	6.62mA	
137	**Gnd**	6.62mA	

Table 21: Supply of SCA line buffer

7.4.d) Digital part

This part relates to the generation and the powering of the signals necessary to the writing & reading phases of the SCA.

N° Pin	Name	I dc	Description
62	Vdd	343.3uA	Vdd&Gnd for the LVDS receivers & CSA write clock block
63	Gnd	343.3uA	
65	Vdd	0mA	Vdd&Gnd for the CSA logic part
64	Gnd	0mA	

Table 22: Supply of the digital part

7.5 Polarization of the output buffer

This part relates to the buffering of the analog data in the read phase. It's include the 2 group buffers and output buffer of the SCA block (in amount of the differential output buffer), and the differential output buffer.

N° Pin	Name	I dc	Description
72	Vdd_out	16.03mA (15mA from differential output buffer)	Vdd&Gnd for the Readout buffer & SCA group buffers (configuration: Vgg1=2mA&Vgg7=1mA)
75	Gnd	16.03mA (15mA from differential output buffer)	

Table 23: Supply of the readout buffers

8. The reference D.C voltages and currents

8.1 The reference D.C voltages

The operation of chip AFTER requires a certain number of D.C voltages, controlled and defined on the ***FEC***. These voltages are:

- D.C voltage of the CSA outputs,
- D.C voltage of the CR & SK filter outputs,
- D.C voltage of the Gain-2 outputs,
- D.C voltage at the input of the Gain-2 & reference voltage for the SCA memory cells,
- D.C input & output common voltage of the readout buffer.

All these potentials are defined on the ***FEC***, and could be realized as shown in the Fig.16.

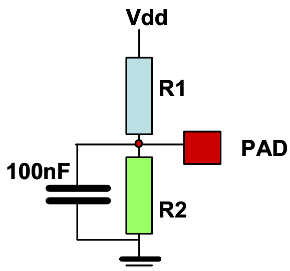


Fig.16: Example of reference voltage building

8.1.a Potential d.c for the CSA output

N° Pin	*Name*	*Vdc*	*I dc*	*Description*
133	Vdc_csad	*2V (+/- 2%)*	*0mA*	*d.c output level voltage of the CSA [37 to 72]*
148	Vdc_csag	*2V (+/- 2%)*	*0mA*	*d.c output level voltage of the CSA [36 to 1]*

Table 24: potential d.c for CSA

8.1.b Potential d.c for the CR & SK filter outputs

N° Pin	*Name*	*Vdc*	*I dc*	*Description*
134	Vdc_cd	*2.2V (+/- 2%)*	*0mA*	*d.c output level voltage of the CR & SK filters [37 to 72]*
147	Vdc_cg	*2.2V (+/- 2%)*	*0mA*	*d.c output level voltage of the CR & SK filters [36 to 1]*

Table 25: potential d.c for the CR & SK filters

The chip AFTER must be able to treat signals of positive polarity (TPC of T2K) or negative. We must consequently adapt the level of tension D.C of the electronics to the polarity of the detector signal. This adaptation is made by changing the level of the tensions defined on the FEC. For T2K, the potential D.C is of 2.2V; 0.7V for the opposite polarity.

8.1.c Potential d.c for the Gain-2 output

N° Pin	Name	Vdc	I dc	Description
135	Vdc_g2d	0.7V (+/- 2%)	0mA	d.c output level voltage of the Gain-2 [37 to 72]
146	Vdc_g2g	0.7V (+/- 2%)	0mA	d.c output level voltage of the Gain-2 [36 to 1]

Table 26: potential d.c for Gain-2

For T2K, the potential is 0.7V; 2.2V for the opposite polarity.

8.1.d Potential d.c for the input of Gain-2 & reference for the SCA

N° Pin	Name	Vdc	I dc	Description
138	Vref_scad	0.7V (+/- 2%)	0mA	d.c input level voltage of the Gain-2 [37 to 72] & reference voltage of the memory cells (Vreturn)
142	Vref_scag	0.7V (+/- 2%)	0mA	d.c input level voltage of the Gain-2 [36 to 1] & reference voltage of the memory cells (Vreturn)

Table 27: potential d.c for Gain-2 & reference for SCA

8.1.e D.C input common voltage for the readout buffer

N° Pin	Name	Vdc	I dc	Description
71	Vicm	1.45V (+/- 2%)	[Vop – Vicm]/11 .638KΩ	Common mode input voltage for readout buffer

Table 28: D.C input common voltage for the readout buffer

Instead of the other reference voltages, a current must be delivered or absorbed by the external supply (Fig.17). The value is given by:

[Vop – Vicm] /11 .638KΩ; maximal value equal to +60uA/- 26uA.

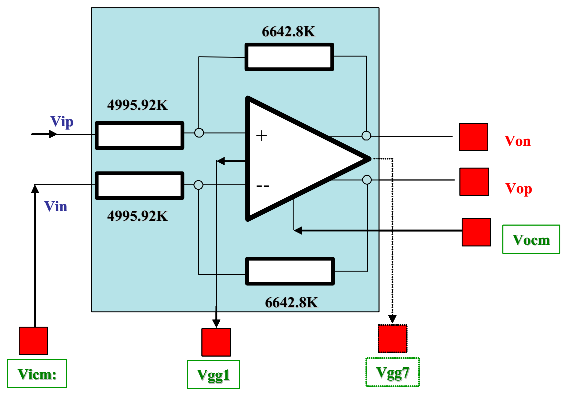


Fig.17: schematic of the readout buffer

8.1.f D.C common mode output voltage for the readout buffer

N° Pin	Name	Vdc	I dc	Description
68	Vocm	VddADC/2	0mA	Common mode output voltage of the readout buffer

Table 29: D.C common mode output voltage for the readout buffer

8.2 The reference D.C currents.

The operation of chip AFTER requires a certain number of D.C currents for:

- Input transistor of the CSA,
- Input & output stages of the readout buffer.

All these currents are defined on the FEC (Fig.18).

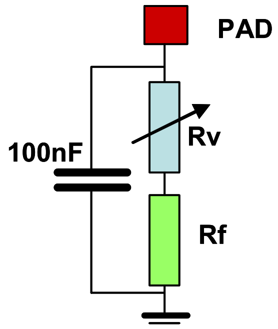


Fig.18: basic schematic of d.c currents

8.2.a Input transistor current of the CSA

N° Pin	*Name*	*I dc*	*Description*
126	Ipol_csad	*note*	*Current supply of the CSA input transistor [37 to 72]*
155	Ipol_csag	*note*	*Current supply of the CSA input transistor [36 to 1]*

Table 30: current for the CSA

The value of this current is a parameter for optimizing the resolution. The range will be between 200uA and 1mA.

8.2.b Input & output stage currents of the readout buffer.

N° Pin	*Name*	*I dc*	*Description*
69	Vgg1	*2mA*	*Current bias of the input stage of the Readout buffer*
70	Vgg7	*1mA*	*Current bias of the output stage of the Readout buffer*

Table 31: input & output currents for the readout buffer

These currents optimize the settling time of the output signal.

9. The main characteristics

In this chapter are presented the main performances expected for the first version of the chip AFTER. All these data obtained by simulation give a reference that will be useful when the test on the chip will be done.

9.1 The power dissipation

The power dissipation is an important parameter for the temperature control at the level of the TPC chambers.

In the normal mode, the total power is around: 5mW + 3.3xIpolcsa. According to the value of the CSA input transistor taken, the power dissipation will be between ***5.66mW*** and ***8.3mW***.

This power dissipation can be reduced by using the alternated power down mode. This mode puts the SCA line buffer in the power down mode during the writing phase, and next a great part of the analog channel (CR & SK filters and Gain -2) during the reading phase. The power dissipation will be between ***4.46mW*** and ***7.1mW***.

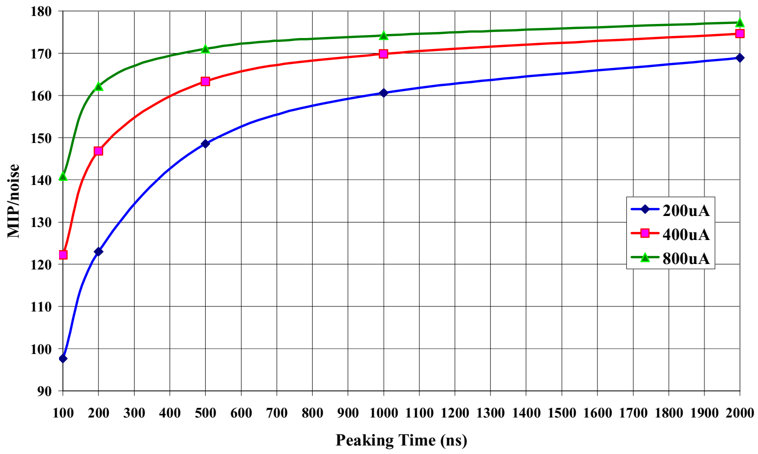
9.2 The resolution on the energy measurement.

The resolution on energy measurement depends:

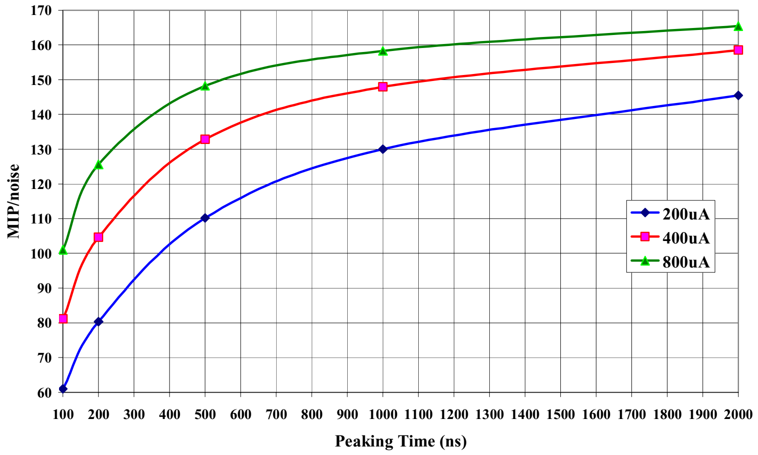
- Value of the input capacitor. The input capacitor is a sum of capacitors coming from the detector pad, input protection diodes, connector, package, and routing path. The maximum expected value is around 20pF to 30pF.
- Value of the peaking Time. The peaking time of the filter is not firstly dedicated to reduce the noise, but essentially to perform the best shaping compatible with a good precision (in time domain) on the z axis measurement. The value will be dependant on the drift velocity of the chamber. More the value of the peaking time is small, more the contribution of the CSA is important.
- Value of the energy range. The contribution of the CSA is inversely proportional to the energy range chosen. This choice will depend on the real gain of the TPC chamber (120fC, 240fC, 360fC or 600fC for the full range).

The uncertainty on the values of the gain & drift velocity of the TPC chamber and the importance of the CSA contribution have involve the possibility to control the current of the CSA input transistor (Ipol_csa). The following graphs show the MIP to noise ratio according to the values of the peaking time, input capacitor, energy range and CSA current.

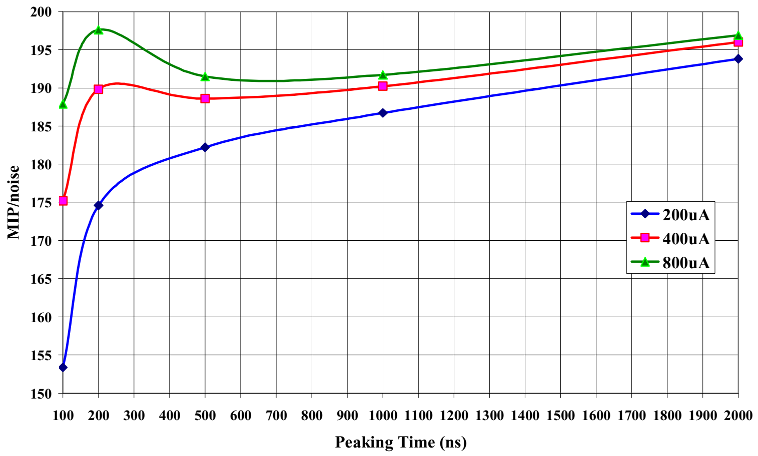
Résolution: Gamme 120fC & Cdét=15pF



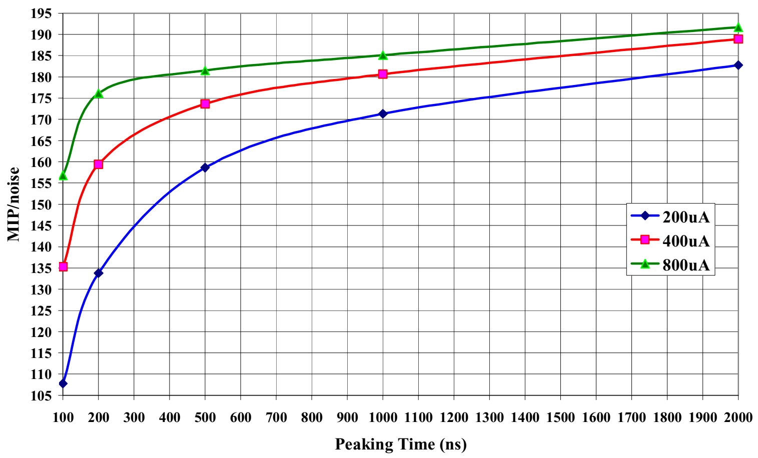
Résolution: Gamme 120fC & Cdét=30pF



Résolution: Gamme 240fC & Cdét=15pF



Résolution: Gamme 240fC & Cdét=30pF



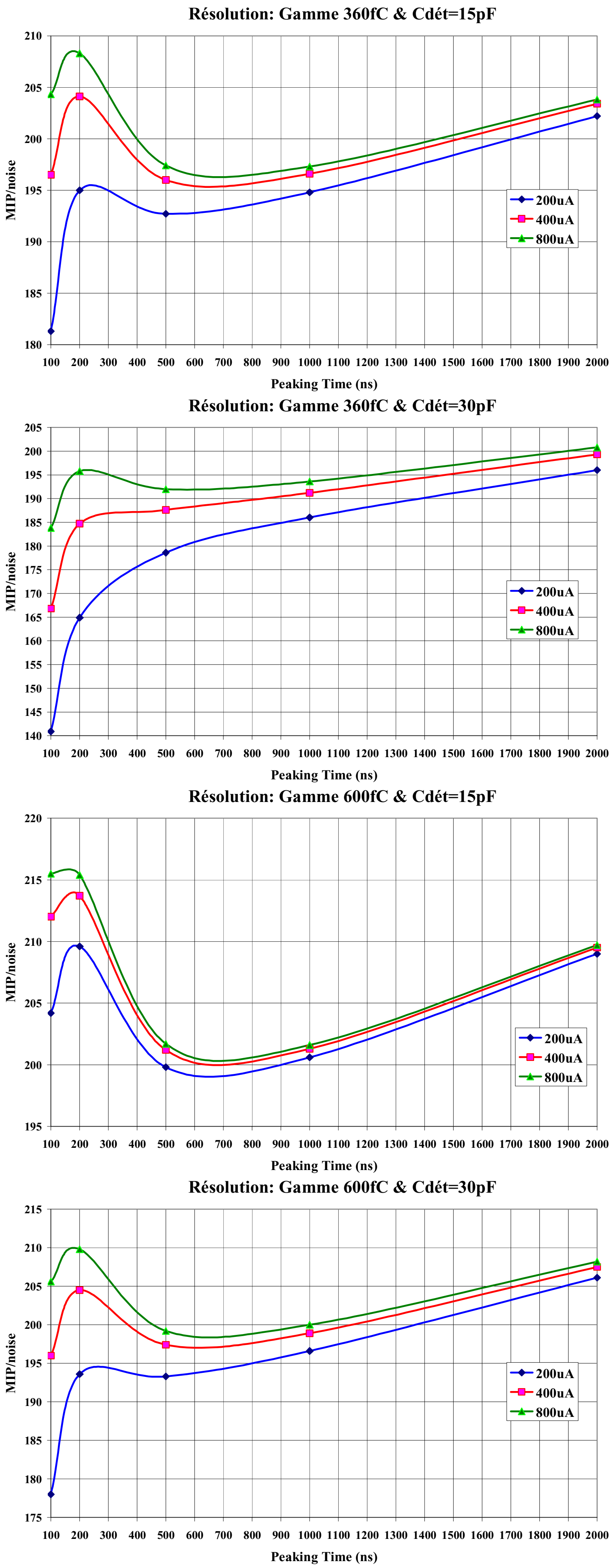


Fig.19: MIP to noise ration versus peaking time

The Fig.19 show that for the range 240fC, 360fC & 600fC the margins are enough compared with the ratio of 100 asked. For the range 120fC, the specification will be obtained by increasing the current in the CSA input transistor and by working with a peaking time greater than 100ns.

9.3 The shape of the signal.

The SCA write frequency will be imposed by the drift velocity of the TPC chamber (Fwrite = 511 x Vdrift/Ldrift). The peaking time of the filter must be compatible with the SCA write frequency to offer a number of samples enough to obtain a good resolution in the measurements of amplitude (energy information) and peaking time (localization on z axis).

The filter used is a CR-RC^2. The shape of the signal (Fig.20) presents some characteristics that will be taken into account for its digitization.

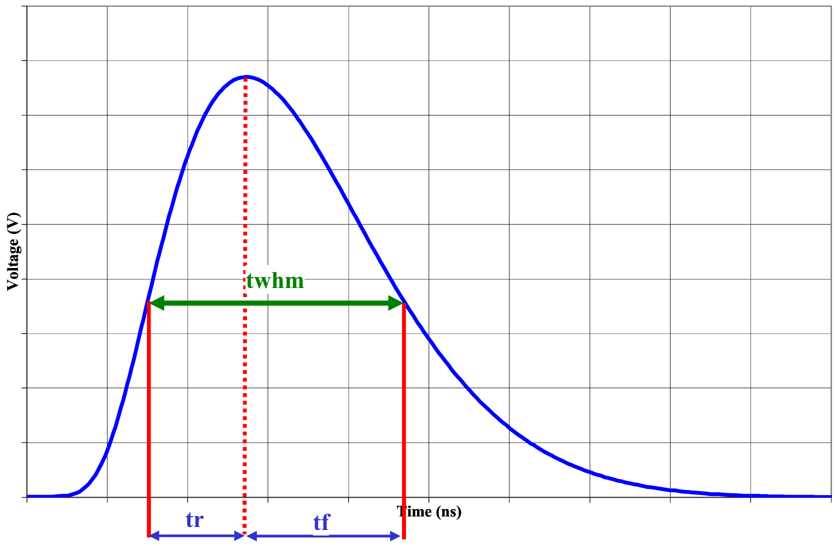


Fig. 20: Shape of the filtered signal

These characteristics are summarized in the table 32.

Tpeak theoretical	*Tpeak measured*	*twhm*	*tr*	*tf*
100ns	172.6ns	160.1ns	68.69ns	91.42ns
200ns	269.6ns	308.8ns	122.7ns	186ns
500ns	605.6ns	830ns	323.3ns	506.7ns
1000ns	1157ns	1663ns	649.6ns	1014ns
2000ns	2197ns	3167ns	1252ns	1915ns

Table 32: Occupancy time of the filtered signal

10 Pin configuration and function descriptions

The significant number of channels (72 in writing, 76 in reading) and the architecture selected (2 groups of 72 (76) channels) brought to obtain a total number of pins equal to 160.

The AFTER chip is packaged in a 160-pin Low Quad Flat Pack (LQFP-160). The package body dimensions are 28 x 28 x 1.4 mm. The pitch is 0.65mm and 2 mm for the footprint.

The pin description of the chip AFTER is indicated in the Fig.21 & table 33.

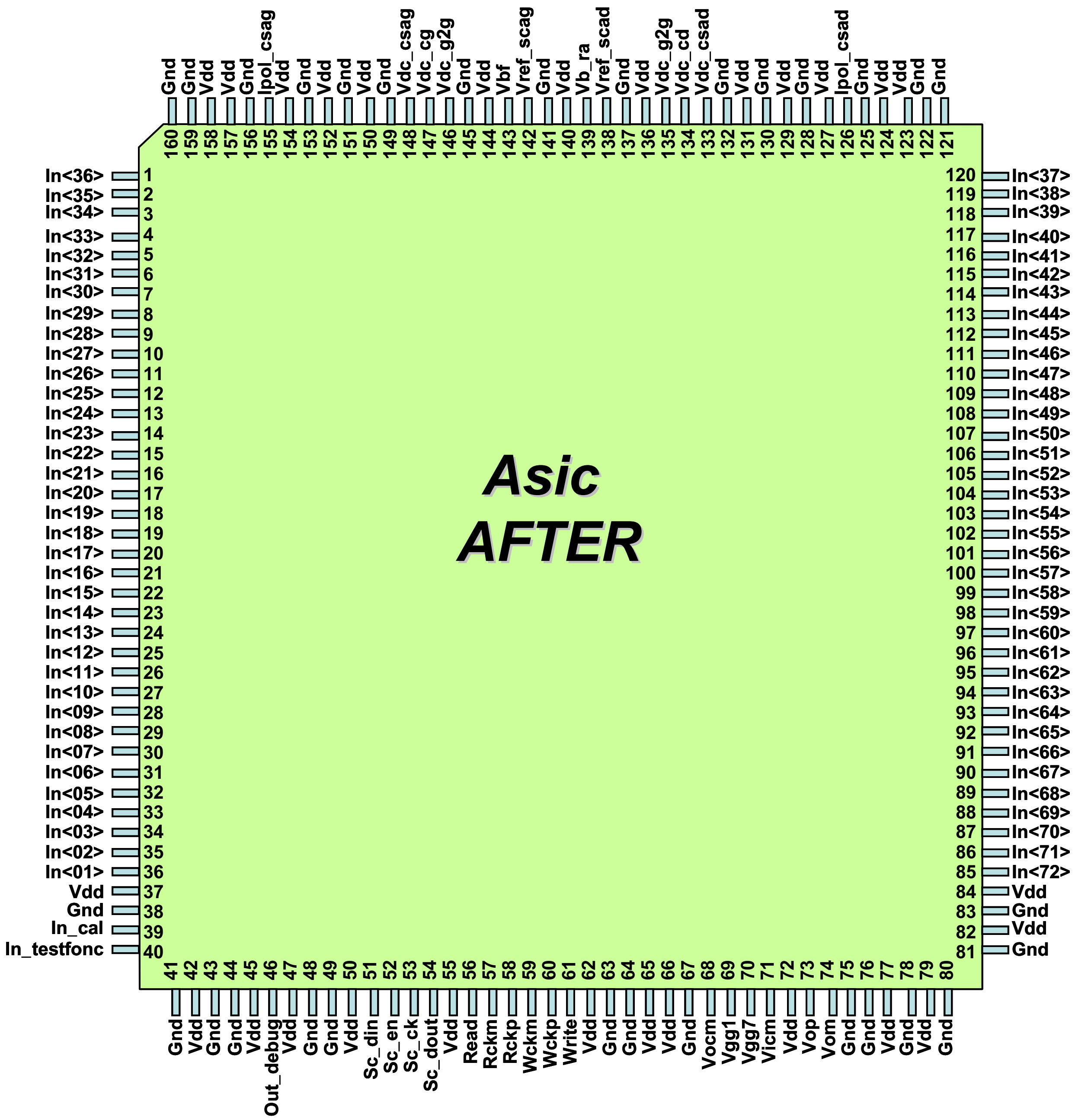


Fig.21: View of the AFTER pin configuration

N° Pin	Name	Dir.	Level	Description
1 to 36	In<36> to In<1>	In	Analog	Inputs of channels 36 to 1
37	Vdd_csag	In	3.3V	Vdd for the csa of the channels 36 to 1
38	gnd	In	0V	Gnd for the csa of the channels 36 to 1
39	In_cal	In	Analog	Input for the calibration
40	In_testfonc	In	Analog	Input for the test & functionality
41	gnd	In	0V	Gnd for protection diode [37 to 84]., cavity , SCA digital part guard ring & Slow Control
42	Vdd_crg	In	3.3V	Vdd for the CR filter of the channels 36 to 1
43	gnd	In	0V	Gnd for the CR filter of the channels 36 to 1
44	gnd	In	0V	Gnd for the SK filter of the channels 36 to 1
45	Vdd_skg	In	3.3V	Vdd for the SK filter of the channels 36 to 1
46	Out_debug	Out	Analog	Output of the "spy" mode
47	Vdd_g2g	In	3.3V	Vdd for the Gain -2 of the channels 36 to 1
48	gnd	In	0V	Gnd for the Gain -2 of the channels 36 to 1
49	gnd	In	0V	Gnd return buffer + Matrix
50	vdd	In	3.3V	Vdd return buffer + Matrix
51	Sc_din	In	CMOS 3.3V	Serial data input of Slow Control
52	Sc_en	In	CMOS 3.3V	Chip Select input of Slow Control
53	Sc_ck	In	CMOS 3.3V	Serial clock input of Slow Control
54	Sc_dout	Out	CMOS 3.3V	Serial data output of Slow Control
55	Vdd_prob	In	3.3V	Vdd for protection diode [37 to 84], SCA digital part guard ring & Slow Control
56	read	In	CMOS 3.3V	SCA read mode
57	rckm	In	LVDS	SCA Negative read clock
58	rckp	In	LVDS	SCA Positive read clock
59	wckm	In	LVDS	SCA Negative write clock
60	wckp	In	LVDS	SCA Positive write clock
61	write	In	CMOS 3.3V	SCA write mode
62	vdd	In	3.3V	Vdd LVDS receiver & block SCA Write Clock
63	gnd	In	0V	Gnd LVDS receiver & block SCA Write Clock
64	gnd	In	0V	Gnd SCA logic
65	vdd	In	3.3V	Vdd SCA logic
66	vdd	In	3.3V	Vdd SCA Readout Amplifier + Matrix
67	gnd	In	0V	Gnd SCA Readout Amplifier + Matrix
68	vocm	In	VddADC/2	Common mode output voltage of the Readout buffer
69	Vgg1	Out	Current 2mA	Current bias of the input stage of Readout buffer
70	Vgg7	Out	Current 1mA	Current bias of the output stage of Readout buffer
71	vicm	In	1.45V mean	Common mode input voltage of the Readout buffer
72	Vdd_out	In	3.3V	Vdd of the Readout buffer & SCA buffer
73	vop	Out	Analog	Positive output of the Readout buffer
74	vom	Out	Analog	Negative output of the Readout buffer
75	gnd	In	0V	Gnd buffer out + logic
76	gnd	In	0V	Gnd for the Gain -2 of the channels 37 to 72
77	Vdd_g2d	In	3.3V	Vdd for the Gain -2 of the channels 37 to 72
78	gnd	In	0V	Gnd for the SK filter of the channels 37 to 72
79	Vdd_skd	In	3.3V	Vdd for the SK filter of the channels 37 to 72
80	gnd	In	0V	Gnd for cavity

N° Pin	Name	Dir.	Level	Description
81	gnd	In	0V	Gnd for the CR filter of the channels 37 to 72
82	Vdd_crd	In	3.3V	Vdd for the CR filter of the channels 37 to 72
83	gnd	In	0V	Gnd for the CSA of the channels 37 to 72
84	Vdd_csad	In	3.3V	Vdd for the CSA of the channels 37 to 72
85 to 120	In<72> to In<37>	In	Analog	Inputs of channels 72 to 37
121	gnd	In	0V	Gnd for cavity
122	gnd	In	0V	Gnd for protection diode [37 to 72]
123	Vdd_proind	In	3.3V	Vdd for protection diode [37 to 72]
124	Vdd_csad	In	3.3V	Vdd for the CSA of the channels 37 to 72
125	gnd	In	0V	Gnd for the CSA of the channels 37 to 72
126	Ipol_csad	Out	Current	Current supply of the input transistors of CSA [37 to 72]
127	Vdd_crd	In	3.3V	Vdd for the CR filter of the channels 37 to 72
128	gnd	In	0V	Gnd for the CR filter of the channels 37 to 72
129	Vdd_skd	In	3.3V	Vdd for the SK filter of the channels 37 to 72
130	gnd	In	0V	Gnd for the SK filter of the channels 37 to 72
131	Vdd_g2d	In	3.3V	Vdd for the Gain -2 of the channels 37 to 72
132	gnd	In	0V	Gnd for the Gain -2 of the channels 37 to 72
133	Vdc_csad	In	2V typ.	d.c output level voltage of the CSA [37 to 72]
134	Vdc_cd	In	2.2V [0.7V]	d.c output level voltage of the CR & SK filters [37 to 72]
135	Vdc_g2d	In	0.7V [2.2V]	d.c output level voltage of the Gain -2 [37 to 72]
136	Vdd	In	3.3V	Vdd SCA Readout Amplifier + Matrix
137	gnd	In	0V	Gnd SCA Readout Amplifier + Matrix
138	vref_scad	In	0.7V	d.c reference level voltage of the SCA
139	vb_ra	in/out	analog	Current source voltage of the internal readout buffer; Control purpose
140	vdd_proh	In	3.3V	Vdd for protection diode [124 to 157]
141	gnd	In	0V	Gnd for protection diode [124 to 157]
142	vref_scag	In	0.7V	d.c reference level voltage of the SCA
143	vbf	in/out	analog	Current source voltage of the Matrix return bus
144	Vdd	In	3.3V	Vdd return buffer + Matrix
145	gnd	In	0V	Gnd return buffer + Matrix
146	Vdc_g2g	In	0.7V [2.2V]	d.c output level voltage of the Gain -2 [36 to 1]
147	Vdc_cg	In	2.2V [0.7V]	d.c output level voltage of the CR & SK filters [36 to 1]
148	Vdc_csag	In	2V typ.	d.c output level voltage of the CSA [36 to 1]
149	gnd	In	0V	Gnd for the Gain 2 of the channels 36 to 1
150	Vdd_g2g	In	3.3V	Vdd for the Gain 2 of the channels 36 to 1
151	gnd	In	0V	Gnd for the SK filter of the channels 36 to 1
152	Vdd_skg	In	3.3V	Vdd for the SK filter of the channels 36 to 1
153	gnd	In	0V	Gnd for the CR filter of the channels 36 to 1
154	Vdd_crg	In	3.3V	Vdd for the CR filter of the channels 36 to 1
155	Ipol_csag	Out	Current	Current supply of the input transistors of CSA [36 to 1]
156	gnd	In	0V	Gnd for the CSA of the channels 36 to 1
157	Vdd_csag	In	3.3V	Vdd for the CSA of the channels 36 to 1
158	Vdd_proing	In	3.3V	Vdd for protection diode [36 to 1]
159	gnd	In	0V	Gnd for protection diode [36 to 1]
160	gnd	In	0V	Gnd for cavity

Table 33: Pin description

11 Chip layout

The integrated circuit is fabricated in AMS CMOS 0.35 µm technology. The silicon area is 7800 µm x 7400 µm for 500,000 transistors used. The number of pads is 160.

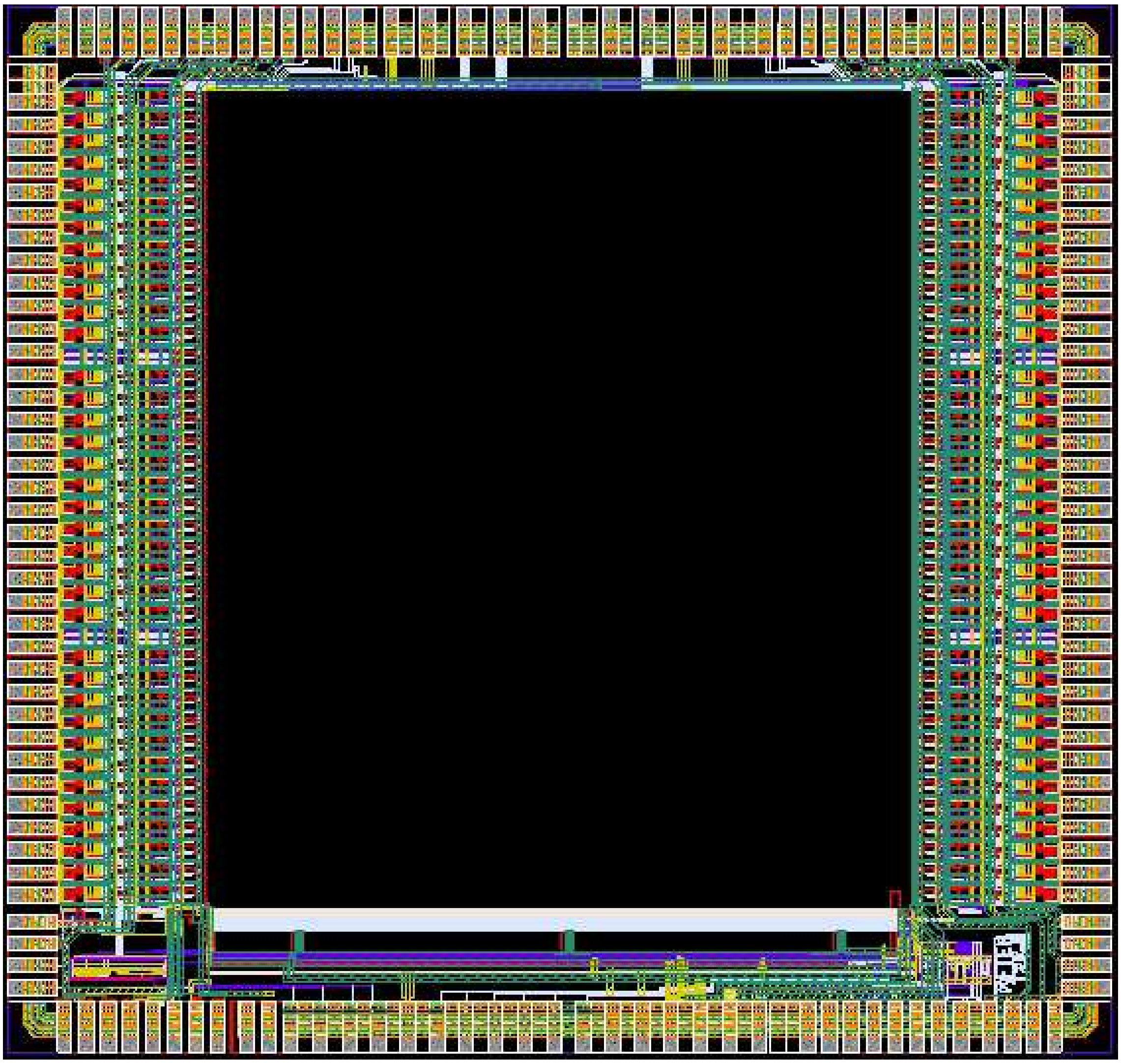
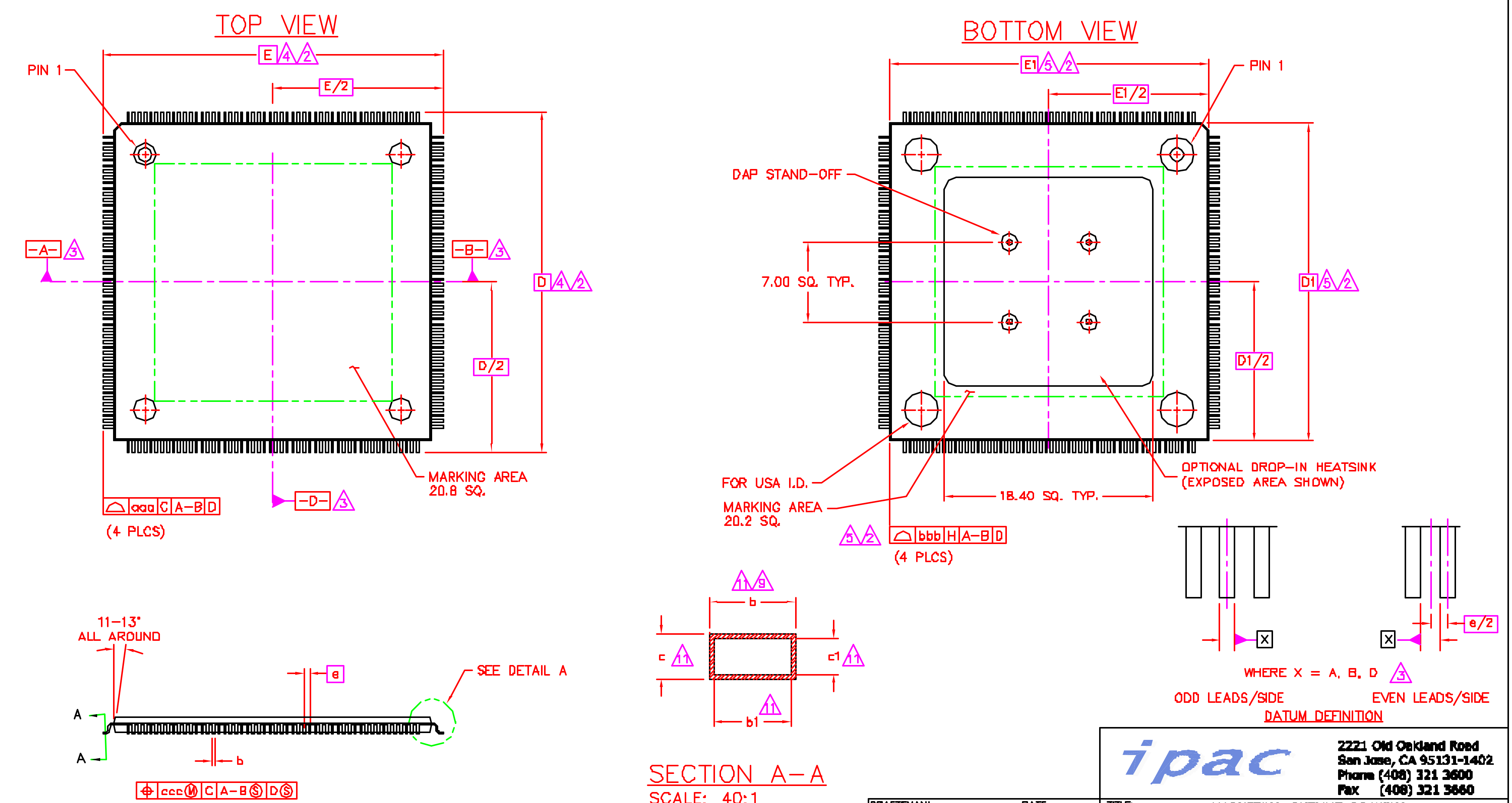


Fig.22: Layout of the chip AFTER

ANNEXE 1 :

Description of the package

REVISION HISTORY			
ECN #	REV	DATE	DESCRIPTION
96-030	A	07/25/96	NEW DRAWING
	B	7/01/98	STAND-OFF(A,A1), CALL-OUT(D,D1,E,E1)ETC. ADD HEATSINK FIGURE
	C	08/11/98	ADD 256 LD, UPDATE NOTES & SPEC.



DRAFTSMAN: Louie Pazonable	DATE 7/01/98	TITLE: MARKETING OUTLINE DRAWING 28 X 28 X 1.4mm LQFP UNIVERSAL DIE UP/DOWN	
CHECKER: Dennis Leung	DATE 8/11/98		
APPROVED:	DATE	DRAWING NO.: QFP-MPO-28T-XXX-01	REV. C · PAGE: 1/2 · SCALE:
APPROVED:	DATE		

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REVISION HISTORY			
ECN #	REV	DATE	DESCRIPTION
96-030	A	07/25/96	NEW DRAWING
	B	7/01/98	STAND-OFF(A,A1), CALL-OUT(D,D1,E,E1)ETC. ADD HEATSINK FIGURE
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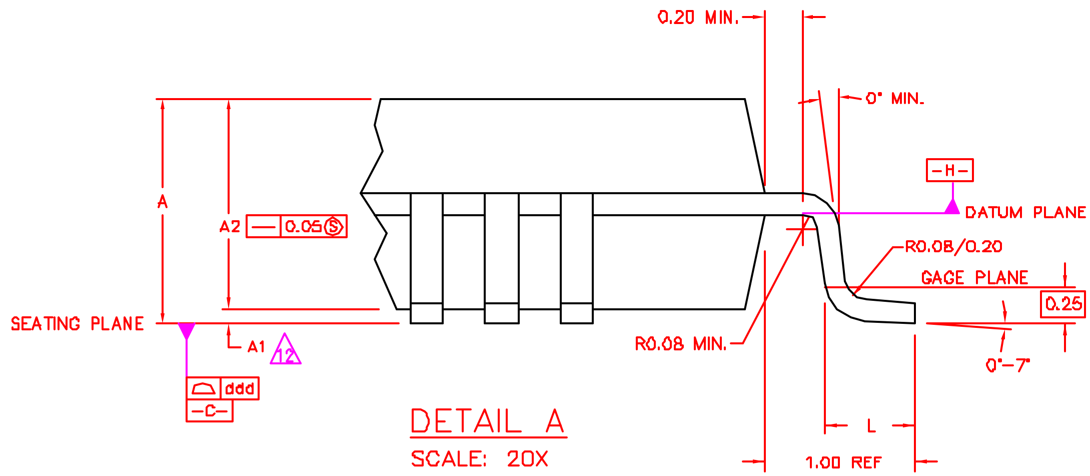

DETAIL A

SCALE: 20X

SYMBOL	LEAD COUNT; FOOT PRINT 160; 2.0 FP			NOTE
	MIN.	NOM.	MAX.	
A	---	---	1.60	
A1	0.05	---	0.15	
A2	1.35	1.40	1.45	
D	30.00 BSC			
D1	28.00 BSC			
E	30.00 BSC			
E1	28.00 BSC			
L	0.45	0.60	0.75	
e	0.65 BSC			
b	0.22	===	0.38	
b1	0.22	0.28	0.33	
c	0.09	===	0.20	
c1	0.09	---	0.16	
	Tolerances of form and position			
aaa	0.20			
bbb	0.20			
ccc	0.12			
ddd	0.08			

SYMBOL	LEAD COUNT; FOOT PRINT 208; 2.0 FP			NOTE
	MIN.	NOM.	MAX.	
A	---	---	1.60	
A1	0.05	---	0.15	
A2	1.35	1.40	1.45	
D	30.00 BSC			
D1	28.00 BSC			
E	30.00 BSC			
E1	28.00 BSC			
L	0.45	0.60	0.75	
e	0.50 BSC			
b	0.17	===	0.27	
b1	0.17	0.22	0.24	
c	0.09	===	0.20	
c1	0.09	---	0.16	
	Tolerances of form and position			
aaa	0.20			
bbb	0.20			
ccc	0.08			
ddd	0.08			

SYMBOL	LEAD COUNT; FOOT PRINT 256; 2.0 FP			NOTE
	MIN.	NOM.	MAX.	
A	---	---	1.60	
A1	0.05	---	0.15	
A2	1.35	1.40	1.45	
D	30.00 BSC			
D1	28.00 BSC			
E	30.00 BSC			
E1	28.00 BSC			
L	0.45	0.60	0.75	
e	0.40 BSC			
b	0.13	===	0.23	
b1	0.13	0.16	0.19	
c	0.09	===	0.20	
c1	0.09	---	0.16	
	Tolerances of form and position			
aaa	0.20			
bbb	0.20			
ccc	0.07			
ddd	0.08			

NOTES:

1. ALL DIMENSIONS ARE IN MM. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982.
2. FOR DIE DOWN PACKAGE, THE TOP PACKAGE BODY IS SHOWN IN BOTTOM VIEW AND THE LEADS ARE FORMED UPSIDE DOWN.
3. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-].
4. TO BE DETERMINED AT SEATING PLANE [-C-].
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. SURFACE FINISH OF THE PACKAGE IS #24-27 CHARMILLE (1.6-2.3 μmR_a). PIN 1 AND EJECTOR PIN MAY BE LESS THAN 0.1 μmR_a.
7. DAMBAR REMOVAL: PROTRUSION DOES NOT EXCEED 0.08. INTRUSION DOES NOT EXCEED 0.03.
8. BURR: BURR DOES NOT EXCEED 0.08 IN ANY DIRECTION.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 FOR 0.40 AND 0.50 PITCH PACKAGE.
10. CORNER RADIUS OF PLASTIC BODY DOES NOT EXCEED 0.20.
11. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
13. FINISH OF LEADS IS TIN/LEAD PLATED.
14. ALL SPECIFICATIONS AND DIMENSIONS ARE SUBJECTED TO IPAC'S MANUFACTURING PROCESS FLOW AND MATERIALS.
15. THE PACKAGES DESCRIBED IN THIS DRAWING CONFORM TO JEDEC MS-026A. WHERE DESCREPANCIES BETWEEN THE JEDEC AND IPAC DOCUMENTS EXIST, THIS DRAWING WILL TAKE THE PRECEDENCE.

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APPROVED:	DATE	DRAWING NO.: QFP-MPO-28T-XXX-01	REV. C
APPROVED:	DATE		PAGE: 2/2 SCALE: NONE

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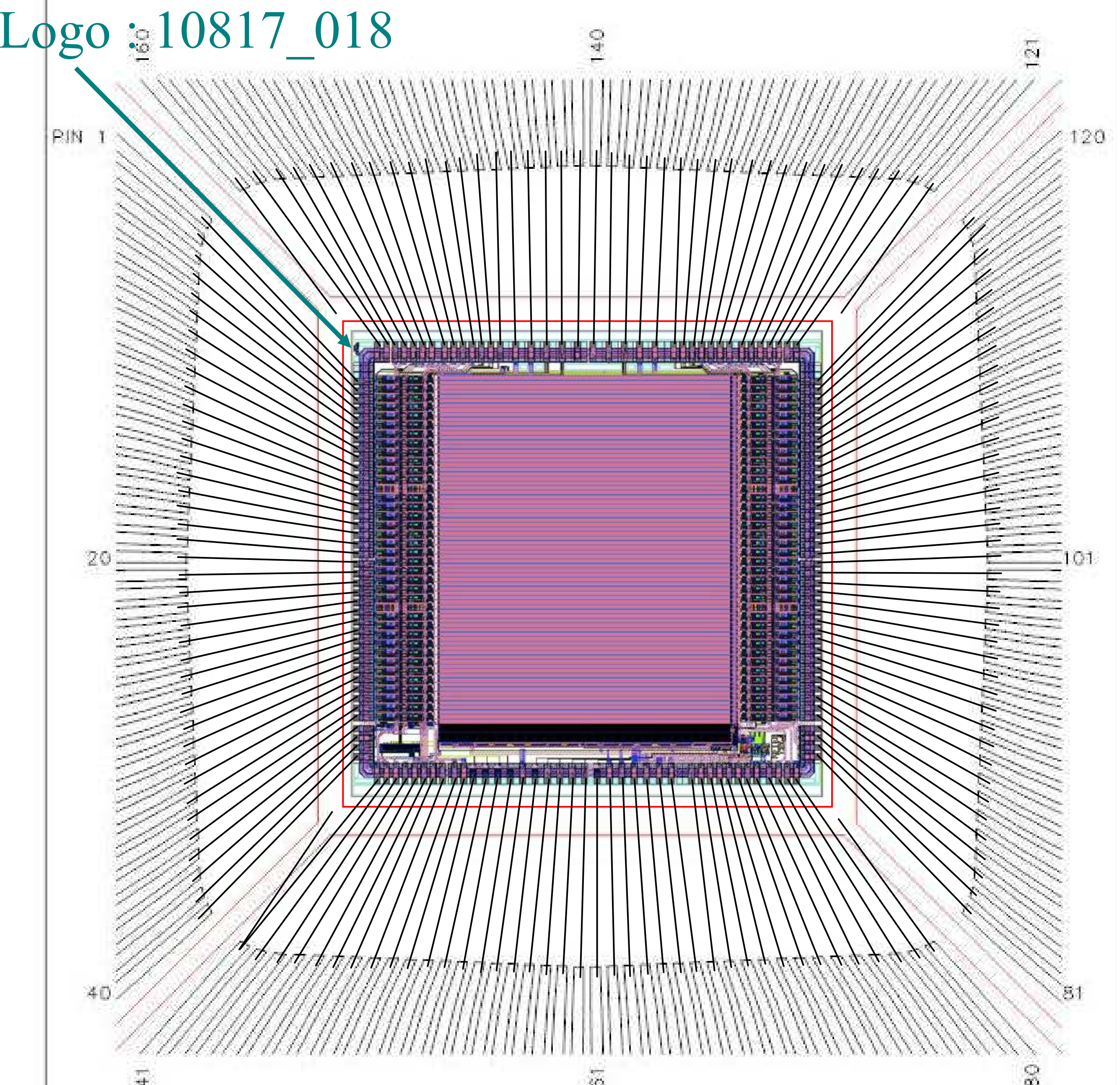
ANNEXE 2:

Bonding diagram

10817_018 – CMP Run A35C6_3



Be careful: - pins package # 41, 80, 121, 160 connected to the cavity (leadframe)

- double bonding on pin package #41

√ CHECK PIN 1
DIE ORIENTATION
WITH RESPECT
TO WAFER FLAT

ECN#	REV.	DESCRIPTION	DATE
98-121	A	NEW RELEASE	04/28/98
00-158	B	CHANGED SCALE TO 1X	08/09/00

DRAWN: DATE: 28/08/2002
CHECKED: DATE: 28/08/2002
APPROVED: DATE:
APPROVED: DATE:

DWG. NUMBER: QFP-BD-2850-160-01

LEADFRAME: LF1-A160-202

D/A PAD SIZE: 7.6mm X 7.6mm

SCALE: DO NOT SCALE DRAWING

TITLE: BOND SHELL – 28 X 28 X 3.4 QFP, 160 LD

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